MSC8156/MSC8156E
Broadband Wireless Access DSP

Advanced 45 nm, six-core DSP for 3G-LTE, TDD-LTE, WiMAX, 3GPP-HSPA and TD-SCDMA

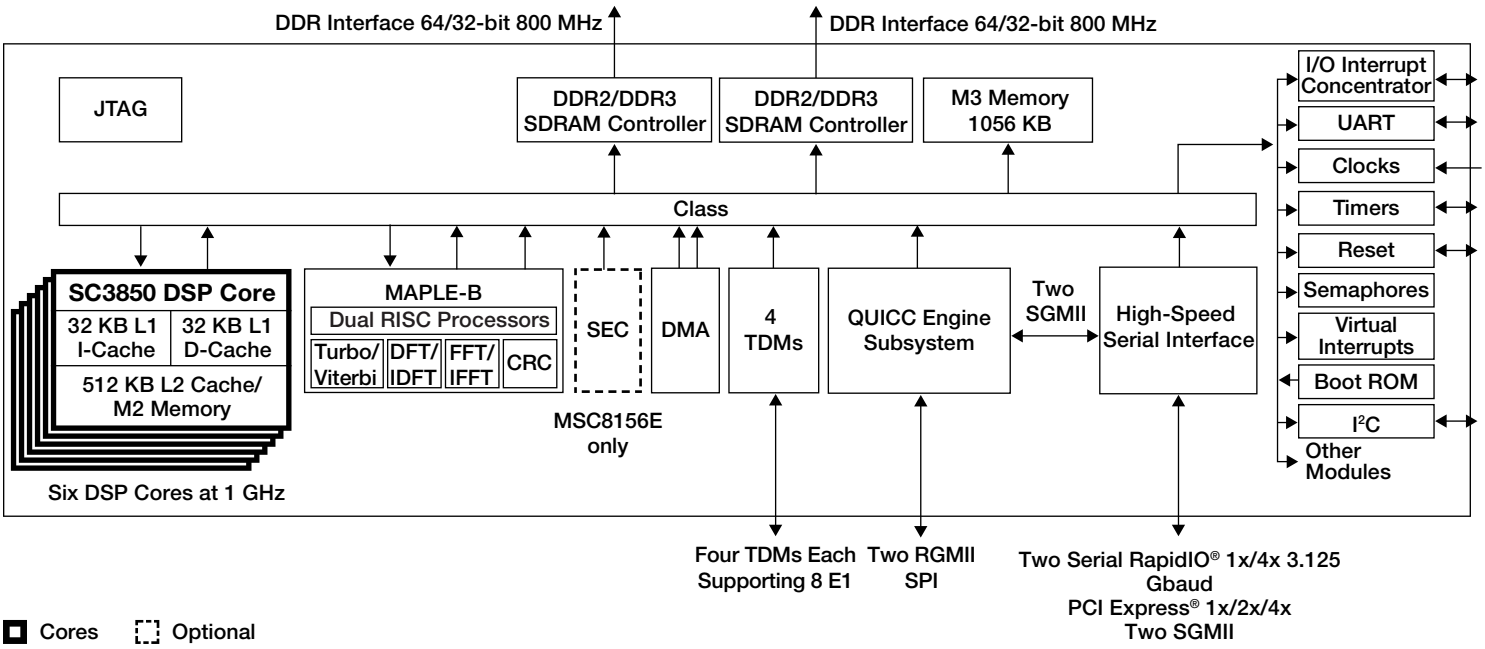
Overview

The MSC8156/MSC8156E is a six-core DSP based on Freescale's new SC3850 StarCore technology and designed to advance the capabilities of wireless broadband equipment. It delivers industry-leading performance and power savings, leveraging 45 nm process technology in a highly integrated SoC to provide performance equivalent to 6 GHz of a single core device. The MSC8156/MSC8156E will help equipment manufacturers and carriers create solutions and services that enable near-term, mainstream adoption of next-generation wireless standards such as 3G-LTE, WiMAX, HSPA+ and TDD-LTE. The device is designed to lower system costs by integrating functionality into a single device that previously required multiple discrete parts.

The MSC8156/MSC8156E DSP delivers a high level of performance and integration, combining six fully programmable new and enhanced SC3850 DSP cores, each running at up to 1 GHz with an architecture highly optimized for wireless infrastructure applications. Developed by Freescale and integrated on chip, the MAPLE-B baseband accelerator supports hardware acceleration for Turbo and Viterbi channel decoding and for DFT/iDFT and FFT/iFFT algorithms. An internal RISC-based QUICC Engine subsystem supports multiple networking protocols to guarantee reliable data transport over packet networks while significantly offloading processing from the DSP cores. The optional security engine core (SEC) in the MSC8156E accelerates data plane encryption/decryption and code protection with minimal DSP core intervention.

The MSC8156/MSC8156E embeds large internal memory and supports a variety of advanced, high-speed interface types, including two Serial RapidIO® interfaces, two Gigabit Ethernet interfaces for network communications, a PCI Express® controller, two DDR controllers for high-speed, industry standard memory interface and four multi-channel TDM interfaces.

MSC8158/MSC8158E Block Diagram



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Features and Benefits

- Six StarCore DSP SC3850 core subsystems operating at up to 1 GHz/8000 MMACS per core and up to 48000 MMACS per device
- Multi-accelerator platform engine for baseband (MAPLE-B)
  - Highly flexible, programmable Turbo and Viterbi decoder supports configurable decoding parameters. It can perform up to 200 Mbps of Turbo decoding (six iterations) or up to 115 Mbps of K = 9 (zero tail) Viterbi decoding
  - FFT/iFFT for sizes 128, 256, 512, 1024 or 2048 points at up to 350 million samples per second
  - DFT/iDFT for sizes up to 1536 points at up to 175 million samples per second
- Two master buses for data transfers from/to the system memory at total throughput up to 50 Gbps
- High-speed, high-bandwidth CLASS fabric arbitrates between the DSP cores and other CLASS masters to M2 memory, M3 memory, DDR controllers, MAPLE-B and the configuration registers
- Two DDR controllers with up to 400 MHz clock (800 MHz data) rate and 32/64-bit DDR2/3 SDRAM data bus. Supports SODIMMs and up to 0.5 GB per controller
- 32-channel DMA controller
- Dual RISC core QUICC Engine subsystem operating at up to 500 MHz provides parallel packet processing independent of the DSP cores
  Supports:
  - Two Gigabit Ethernet controllers supporting RGMII or SGMII
  - Serial peripheral interface
- HSSI that supports two 4x SerDes ports, including:
  - Two Serial RapidIO controllers supporting 1x/4x operation up to 3.125 Gbaud
  - One PCI Express controller that supports 1x/2x/4x operation
  - Multiplexing capability for RapidIO, PCI Express and SGMII signals through the two SerDes ports
- Four TDM interfaces
- UART and I^2C interfaces
- Eight software watchdog timers
- 16 16-bit timers
- Two 32-bit general purpose timers per core for RTOS support
- I/O interrupt concentrator and virtual interrupt support
- Eight hardware semaphores
- 32 GPIO ports multiplexed with interface signals and IRQ inputs
- Optional SEC (MSC8156E) optimized to process all the encryption/decryption algorithms associated with IPsec, IKE, WTLS/WAP, SSL/TLS, AES, DES, RC-4, SNOW-3G and Kasumi for 3G-LTE and 3GPP
- Boot options: Ethernet, Serial RapidIO, I^2C and SPI
- Three input clocks and five PLLs
- JTAG Test Access Port (TAP) and boundary scan architecture designed to comply with IEEE 1149.1™ standard for profiling and performance monitoring support
- Reduced power dissipation with wait, stop and power down low-power standby modes
- Optimized power management circuitry
- Technology: CMOS 45 nm SOI technology in 29 mm, 29 mm, 783 ball, FC-PBGA package

Development Support

Freescale supplies a complete set of CodeWarrior DSP development tools for the MSC8156/MSC8156E device. The tools provide easier and more robust ways for designers to develop optimized DSP systems. Whether the application targets a 3G-LTE, TD-SCDMA or WiMAX system, the development environment gives designers everything they need to exploit the advanced capabilities of the MSC8156/MSC8156E architecture.

Support tools include:

- Eclipse-based integrated development environment (IDE)
- C and C++ compiler with in-line assembly
- Librarian
- Multicore debugger
- Royalty-free RTOS
- Software simulator
- Profiler
- High-speed run control
- Host platform support
- MSC8156ADS development board
- MSC8156EVM evaluation module

Contact your local sales office or representative for availability.

Learn More: For current information about Freescale products and documentation, please visit **freescale.com/DSP.**

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