4:1 ActiveEye™ HDMI™ Switch with Electrical Idle Detect and I²C Control

Features

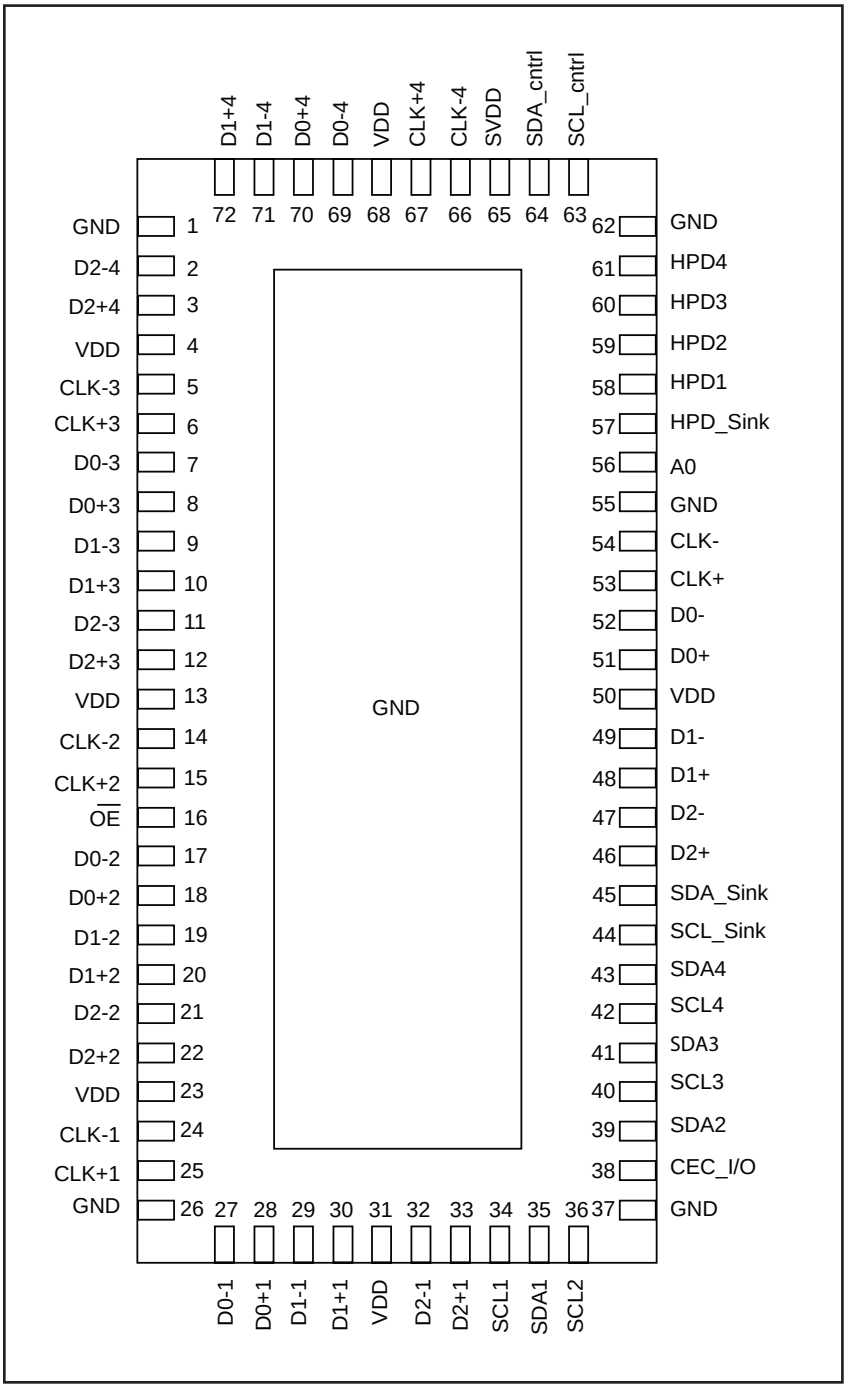
- 4 digital-video inputs can be switched to a single output
- Each input can be AC coupled video or DC coupled, while the output will maintain its DC coupled, current-steering, TMDS compliance
- TMDS pixel clock support up to 250MHz max
- Deep Color™ support up to 36bits max per link
- Integrated DDC switch to connect DDC path from HDMI input connectors to HDCP block in the HDMI Receiver.
- HDCP reset circuitry for quick communication when switching from one port to another
  - → Automatic Termination turn-off circuitry when port is deselected
- Clock Detection: Will disable output TMDS channels when no TMDS pixel clock is present
- Flexible termination;
  - → When TMDS channel is off, 50Ω termination is turned off
- Integrated ESD on all data input channels (Dx+/-y, CLK+/-y, HPDy, CECI/O, SCLy & SDAy)
  - → 8kV contact per IEC61000-4-2, level 4 for Dx+/-y, CLK+/-y, HPDy, SCLy, SDAy, and CEC I/O
- I²C control for IC configuration
- Packaging (Pb-free and Green)
  - → 72-contact TQFN (ZL)

Description

Fully compatible HDMI™ signal support with backward compatibility to the DVI 1.0 standard, Pericom's new "ActiveEye™" switch technology is all you need to connect multiple, unknown sources, to a single display. Without any affect on HDCP, these switches can be used almost anywhere. In addition to supporting DC coupled HDMI and DVI inputs, Pericom's PI3HDMI245-A can also level shift an AC coupled HDMI to a DC coupled HDMI output.

Pericom's HDMI product family has been designed specifically to support color depths of up to 12-bits per channel, as specified in the HDMI revision 1.3 standard. We have integrated the entire interface solution so the TV designer doesn't have to think about it. This includes, integrated DDC switching.

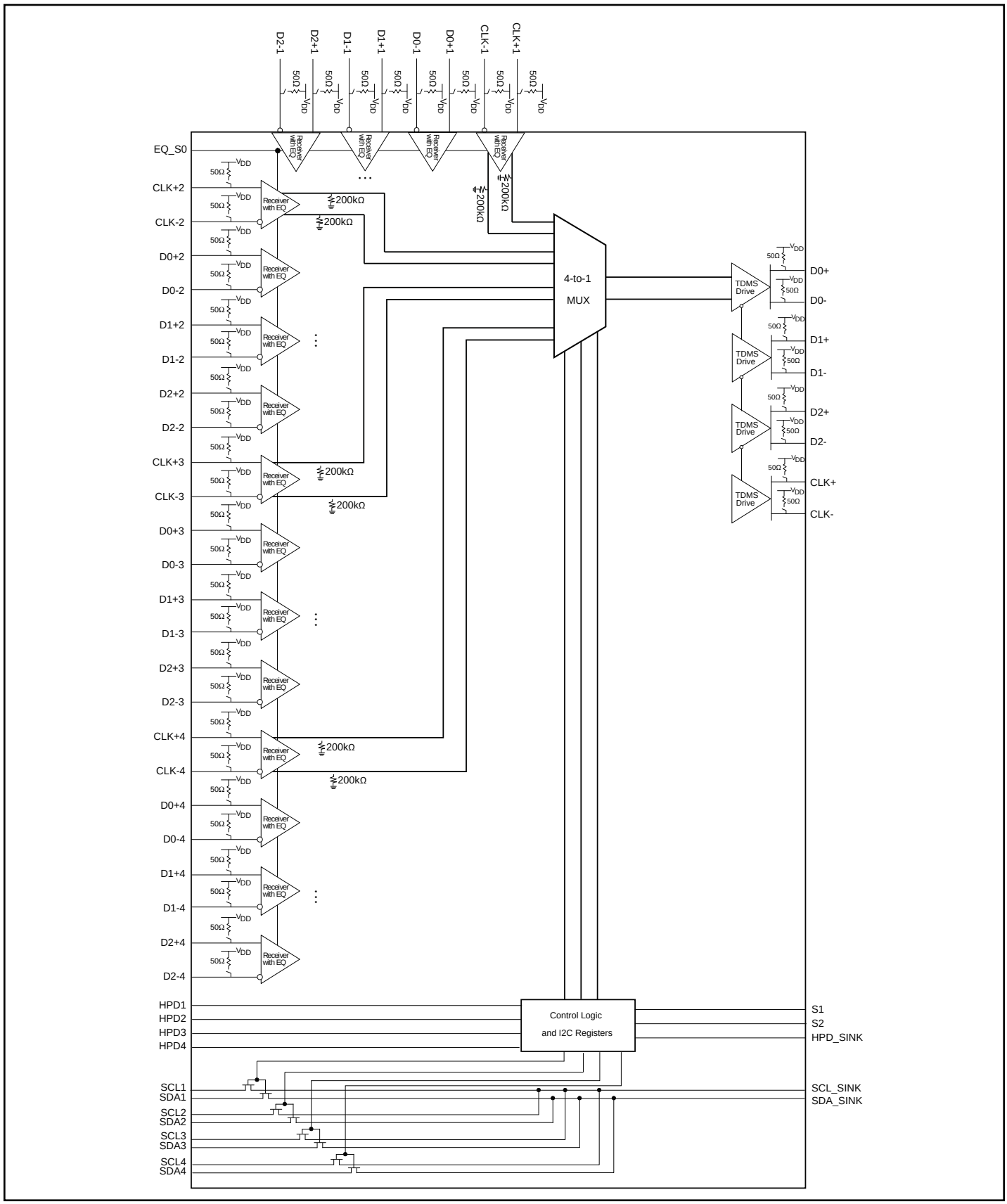
Pin Description



Pin Description

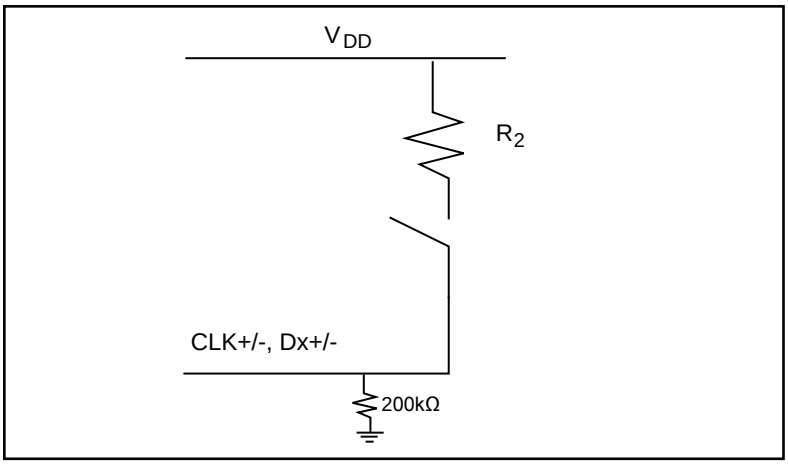
Pin #	Pin Name	Type	Function / Description
3, 8, 10, 12, 18, 20, 22, 28, 30, 33, 70, 71	Dx+y	I	Positive TMDS data inputs for port y (y = 1, 2, 3, 4)
2, 7, 9, 11, 17, 19, 21, 27, 29, 32, 69, 72	Dx-y	I	Negative TMDS data inputs for port y (y = 1, 2, 3, 4)
25, 15, 6, 67	CLK+y	I	Positive TMDS clock inputs for port y (y = 1, 2, 3, 4)
24, 14, 5, 66	CLK-y	I	Negative TMDS clock inputs for port y (y = 1, 2, 3, 4)
4, 13, 23, 31, 50, 68	VDD	PWR	3.3V Power Supply
1, 26, 37, 55, 62	GND	GND	Ground
16	$\overline{OE}$	I	Output Enable (Active LOW)
34, 36, 40, 42	SCLy	I	DDC clock input for port y
35, 39, 41, 43	SDAy	I/O	DDC data I/O for port y
58, 59, 60, 61	HPDy	O	HPD open drain buffer output for port y (5V tolerant)
38	CEC_I/O	I/O	ESD protection for CEC signal
65	SVDD	PWR	Standby Power Rail, 3.3V to 5V
57	HPD_Sink	I	Determines status of HPD y for chosen port
44 45	SCL_Sink/ SDA_Sink	I/O	Sink side DDC signals
56	A_0	I	I^2C controls address A_0
51, 48, 46	Dx+	O	Positive TMDS data outputs
52, 49, 47	Dx-	O	Negative TMDS data outputs
53	CLK+	O	Positive TMDS clock outputs
54	CLK-	O	Negative TMDS clock outputs
64	SDA_Cntrl	I/O	I^2C control interface data control signal
63	SCL_Cntrl	I	I^2C control interface clock signal

Block Diagram



Receiver Block

The HDMI/DVI receive ports are terminated separately as follows:



Each input has integrated equalization that can eliminate deterministic jitter caused by 20meter 24AWG cables. The Rx block is designed to receive all relevant signals directly from the HDMI connector without any additional circuitry, 3 High speed TMDS data, 1 pixel clock, and DDC signals. EQ control, port selection, + termination control can all be configured through I²C control interface..

Equalizer Truth Table for TMDS data channels only. TMDS clk channels have fixed gain.

EQ_1	EQ_0	EQ value on TMDS data channels
0	0	6dB (default)
0	1	12dB
1	0	2dB
1	1	15dB

I²C Control Block

	Register Bits							
Byte Name	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Address byte	1 R Only	0 R Only	1 R Only	0 R Only	1 R Only	0 R Only	A0 R/W	0/1 (0 indicates write function; 1 indicates read function)
Control byte (byte 0)	ST_ CNTRL R/W	OC3 R/W	OC2 R/W	OC1 R/W	Sink Detec-tion R/W	Squelch enable R/W	S2 R/W	S1 R/W
HPD Control (byte 1)	HPD Control R/W	PD R/W	EQ_1 R/W	EQ_0 R/W	HPD4 R/W	HPD3 R/W	HPD2 R/W	HPD1 R/W

Truth Table for source termination (Bit 7, byte 0)

ST_Cntrl	Output Termination
0	disabled
1	enabled

Truth Table for squelch (Bit 2, byte 0)

Squelch Enable	Function
0	disabled
1	enabled

I²C Bit Explanation

Input Control Pins			**Setting Value**	
OC3	OC2	OC1	Vswing (mV)	Pre-emphasis/De-emphasis (dB)
0	0	0	500 (Default)	0
0	0	1	750	0
0	1	0	1000	0
0	1	1	600	0
1	0	0	500	0
1	0	1	500	1.5
1	1	0	500	3.5
1	1	1	500	6

Port Selection Truth Tab

Selectors		**I/o Selection**	
S2	S1	TMDS Output Port	SCL_SINK/SDA_SINK
H	H	TMDS input Port1 (Port 2, 3, and 4 50Ω termination will be off)	SCL1/SDA1
H	L	TMDS input Port2 (Port 1, 3, and 4 50Ω termination will be off)	SCL2/SDA2
L	L	TMDS input Port3 (Port 1, 2, and 4 50Ω termination will be off)	SCL3/SDA3
L	H	TMDS input port4 (Port 1, 2, and 3 50Ω termination will be off)	SCL4/SDA4

Table: S1, S2 can be controlled through the I²C register, byte 0 bits B0, and B1.

Truth Table for Sink Detection (Bit 3, byte 0)

Sink Detection[1]	**Function**
0	Sink Detection disabled
1	Sink Detection enabled (can only be enabled if source termination is OFF.

Note:
1) If sink detection is enabled, and no sink (50Ω Rx termination) is detected, then PI3HDMI245-A input termination will be disabled automatically.

HPD Control Byte 1 Explanation

When bit B7 (HPD Control) is 0, then HPD_Sink pin (pin 57) is used to determine the status of HPDx signal. When bit B7 (HPD control) is 1, then bits B0, B1, B2 and B3 from byte 1 will be used to determine HPD output buffer status for each port.

Truth table if HPD_Sink is used:

Selectors		**I/o Selection**			
S2	S1	HPD1	HPD2	HPD3	HPD4
H	H	Hi-Z	L	L	L
H	L	L	Hi-Z	L	L
L	L	L	L	Hi-Z	L
L	H	L	L	L	Hi-Z

Truth table if I²C register byte 1 is used (independent of S1/S2 state):

I²C Byte1 (HPD control bits)				Results			
Bit0	Bit1	Bit2	Bit3	HPD1 (pin 58)	HPD2 (pin 9)	HPD3 (pin 60)	HPD4 (pin 61)
0	0	0	0	Low	Low	Low	Low
0	0	0	1	Low	Low	Low	Hi-Z
0	0	1	0	Low	Low	Hi-Z	Low
0	0	1	1	Low	Low	Hi-Z	Hi-Z
0	1	0	0	Low	Hi-Z	Low	Low
0	1	0	1	Low	Hi-Z	Low	Hi-Z
0	1	1	0	Low	Hi-Z	Hi-Z	Low
0	1	1	1	Low	Hi-Z	Hi-Z	Hi-Z
1	0	0	0	Hi-Z	Low	Low	Low
1	0	0	1	Hi-Z	Low	Low	Hi-Z
1	0	1	0	Hi-Z	Low	Hi-Z	Low
1	0	1	1	Hi-Z	Low	Hi-Z	Hi-Z
1	1	0	0	Hi-Z	Hi-Z	Low	Low
1	1	0	1	Hi-Z	Hi-Z	Low	Hi-Z
1	1	1	0	Hi-Z	Hi-Z	Hi-Z	Low
1	1	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z

I²C Power-up Condition

	Register Bits							
Byte Name	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Address byte	1	0	1	0	1	0	A0	0/1
Control byte (byte 0)	0	0	0	0	0	1	0	0
HPD Control (byte 1)	1	0	0	0	0	0	0	0

I²C Read/Write Format

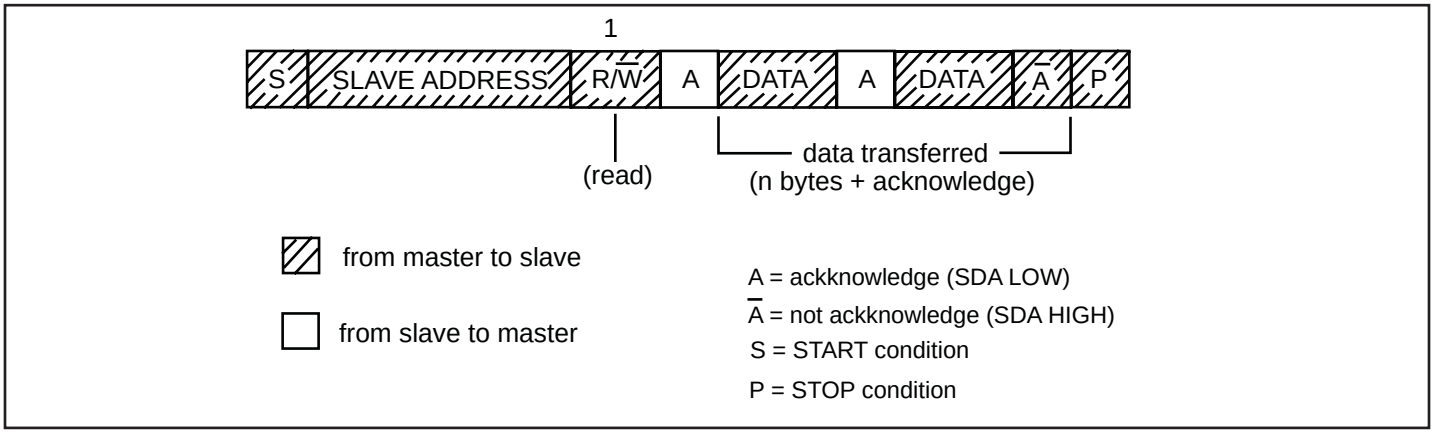


Figure 1: A master transmitter addressing a slave receiver with 7-bit address. The transfer direction is not changed.

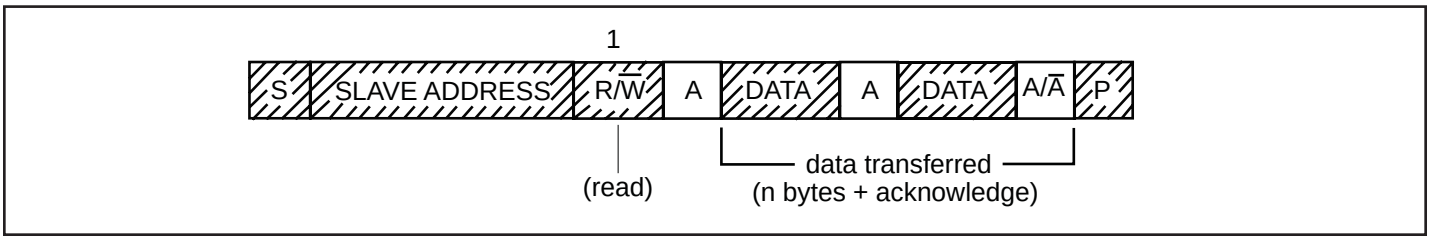


Figure 2: Master reads a slave immediately after the first byte.

WRITE MODE
Start bit → Slave address → W(write) → Offset byte → Data1 → Data2 → ..... Datan → Stop bit

Data will be written to the device pointed by the offset byte first and then the next, until master stops the data stream

READ MODE
Start bit → Slave address → W(write) → Offset byte → Restart bit → Slave address → R(read) → Data1 → Data2 → .....→ Datan → Stop bit

Data will be read from the device pointed by the offset byte first and then the next,... until master stops the data stream.

ABSOLUTE MAXIMUM RATAINGS

Parameter	Comments	Units
Supply Voltage Range, V_{DD}		–0.5 V to 4 V
I^2C control voltage Voltage, SV_{DD}	Needs to be present for I^2C control to operate	-0.5V to 6V
Normal I/O Voltage Range		–0.5 V to 4 V
5V Safe I/O Voltage Range	SCLx, SDAx, HPD_SINK, CEC	–0.5 V to 6 V
ESD	Human Body Model per JESD22 spec (Dx+/-y, CLK+/-y, HPDy, SCLy, SDAy, and CEC I/O)	± 3 kV
	Contact per IEC61000-4-2 Standard (Dx+/-y, CLK+/-y, and CEC I/O)	± 8 kV
	Machine Model: All ins	± 400 V
	Charged Device Mode: All pins	± 2 kV
Power Consumption	T_A = 70°C, Θja = 67.0	738 mW

ESD Standard:
Human Body Mode: JESD22-A114-D
Machine Mode: JESD22-A115-A
Charged Device Mode: JESD22-C101-A
Latch-up Standard: JEDEC STANDARD No. 78A FEBRUARY 2006; Class-I; I-Test and V-Test
Contact: IEC61000-4-2

ELECTRICAL SPECIFICATIONS

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
V_{DD}	TMDS Supply Voltage	-0.3		4.0	V	1, 2
V_I	Input Voltage	-0.3		V_{DD}+0.3	V	1, 2
V_O	Output Voltage	-0.3		V_{DD}+0.3	V	1, 2

Notes:
1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	TMDS Analog Supply Voltage	3.135	3.3	3.465	V
SV_{DD}	+3.3V power supply used to power I²C control and DDC/HPD path	3.0		5.5	V
T_A	Ambient Temperature (with power applied)	0	25	70	°C
TJ	Operating Junction Temperature			125	°C

Electrical Characteristics Over Recommended Operating Conditions (unless otherwise noted)

Symbol	Description	Test Conditions		Min	Typ	Max	Units
$I_{CC\_}V_{DD}$	Supply current	$\overline{OE}$ = LOW and PD = 0	R_T=50Ω, V_{DD}=3.3V TMDS data inputs= 2.25Gbps HDMI data pattern TMDS clock input = 225MHz, pre-emphasis = 0dB		140	180	mA
I_{CCq}	$\overline{OE}$ = HIGH or PD = 1					750	µA
$I_{CC\_}SV_{DD}$	Supply current for SV_{DD}		HPDx has no load			1	mA

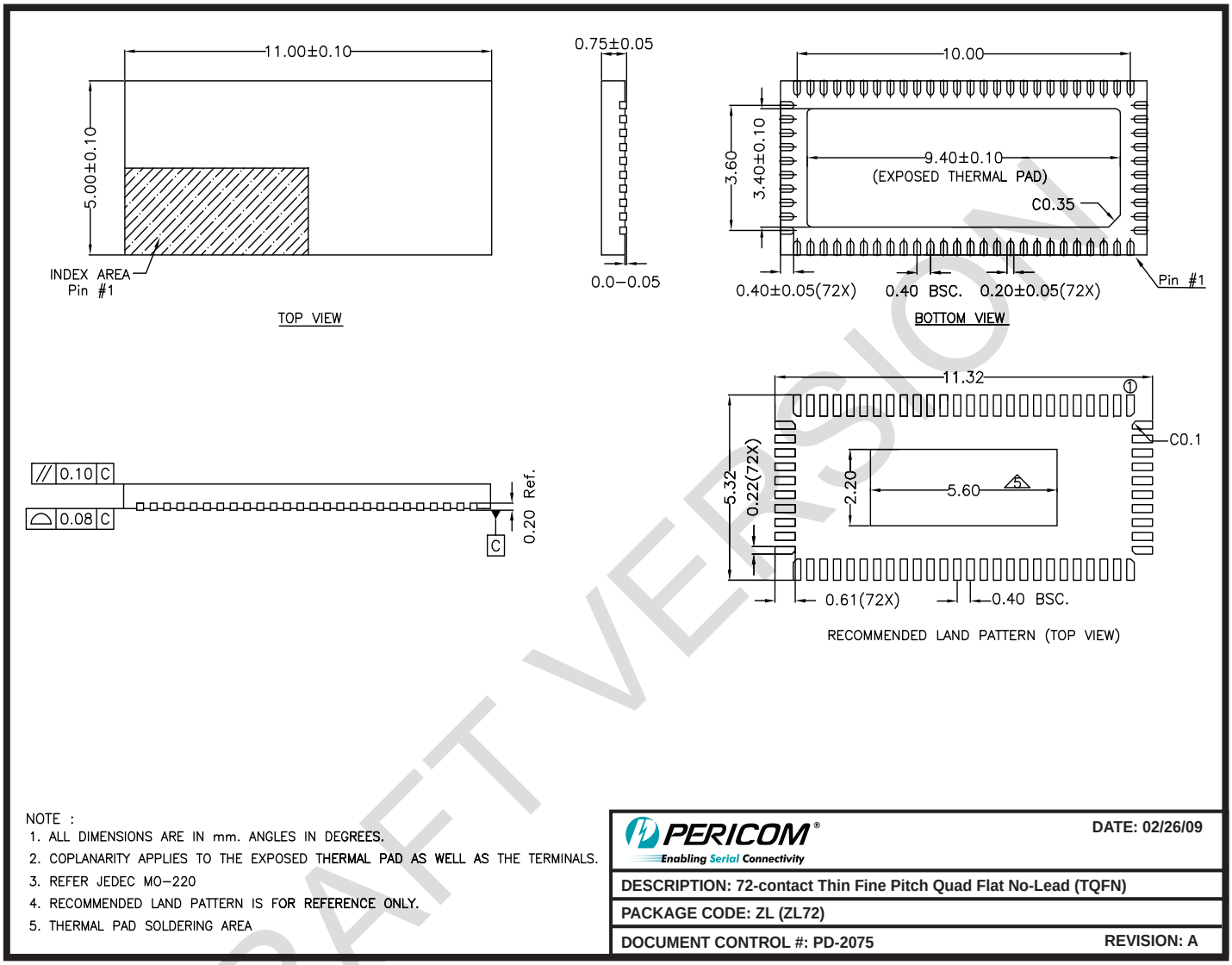
Electrical Characteristics Over Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
TMDS differential pins						
V_{OH}	Single-ended high level output voltage	V_{DD} = 3.3V, R_T = 50Ω	V_{DD}-10		V_{DD}+10	mV
V_{OL}	Single-ended low level output voltage		V_{DD}-600		V_{DD}–400	mV
V_{swing}	Single-ended output swing voltage		400		600	mV
$V_{OD(O)}$	Overshoot of output differential voltage				15%	2 x Vswing
$V_{OD(U)}$	Undershoot of output differential voltage				25%	2 x Vswing
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states				5	mV
I_{OS}	Short Circuit output current		-12		12	mA
$V_{I(open)}$	Single-ended input voltage under high impedance input or open input	I_I = 10uA	V_{DD}-10		V_{DD}+10	mV
R_{INT}	Input termination resistance	V_{IN} = 2.9V	45	50	55	Ω
Clk_Detect	TMDS clock detection for normal operation. Outputs are Hi-Z if CLK signal detected is outside of this Normal operating range	Frequency	15		340	MHz
		Differential Voltage Swing	140			mV
I_{OZ}	Leakage current with Hi-Z I/O	V_{DD} = 3.6V, SV_{DD} = 3.6V			10	µA

Switching Characteristics (over recommended operating conditions unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
TMDS Differential Pins						
tpd	Propagation delay	V_{DD} = 3.3V, R_T = 50Ω			2000	ps
t_r	Differential output signal rise time (20% - 80%)			140		
t_f	Differential output signal fall time (20% - 80%)			140		
$t_{sk(p)}$	Pulse skew			10	50	
$t_{sk(D)}$	Intra-pair differential skew			23	50	
$t_{sk(o)}$	Inter-pair differential skew(2)				100	
$t_{jit(pp)}$	Peak-to-peak output jitter CLK residual jitter	Data Input = 1.65 Gbps HDMI data pattern CLK Input = 165 MHz clock		15	30	
$t_{jit(pp)}$	Peak-to-peak output jitter DATA residual jitter			18	50	
t_{SX}	Select to switch output				10	ns
t_{en}	Enable time				600	
t_{dis}	Disable time				10	
DDC I/O Pins (SCL, SCL_SINK, SDA, SDA_SINK)						
$t_{pd(DDC)}$	Propagation delay from SCLn to SCL_SINK or SDAn to SDA_SINK or SDA_SINK to SDAn	C_L = 10pF		0.4	2.5	ns
Control and Status Pins (OC_SX, EQ_SX, S, HPD_SINK, HPD)						
$t_{pd(HPD)}$	Propagation delay (from HPD_SINK to the active port of HPD)	C_L = 10pF		2	6.0	ns
$t_{sx(HPD)}$	Switch time (from port select to the latest valid status of HPD)			3	6.5	
Control Pins						
I_{IH}	High level digital input current(1)	V_{IH} = 2V or V_{DD}	-40		40	µA
I_{IL}	Low level digital input current(1)	V_{IL} = GND or 0.8V	-40		40	µA
V_{IH}	High level digital input voltage		2.0		SV_{DD}	V
V_{IL}	Low level digital input voltage		0		0.8	V
DDC I/O Pins						
I_{LK}	Input leakage current	V_I = 0.1 V_{DD} to V_{DD} to isolated DDC inputs	-10		10	µA
C_{IO}	Input/Output capacitance	V_I peak-peak = 1V, 100 KHz			10	pF
R_{ON}	Switch resistance	I_O = 3mA, V_O = 0.4V		25	50	Ω
HPD Path						
I_{IH}	High level digital input current	V_{IH} = 2V or V_{DD}	-10		10	µA
I_{IL}	Low level digital input current	V_{IL} = GND or 0.8V	-10		10	µA
V_{OL}	Single-ended low level output voltage	I_{OL} = 4mA	GND		0.4	V
CEC I/O Pin						
I_{OFF}	Leakage current when V_{DD} = 0V	V_{DD} = 0V or open			10	µA

Package Mechanical: 72-pin, Low Profile Quad Flat Package (ZL72)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO–220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA

PERICOM Enabling Serial Connectivity

DATE: 02/26/09

DESCRIPTION: 72-contact Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZL (ZL72)

DOCUMENT CONTROL #: PD-2075 REVISION: A

09-0134

Ordering Information

Ordering Code	Package Code	Package Description
PI3HDMI245-AZLE	ZLE	72-pin, Pb-free & Green TQFN

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X Suffix = Tape/Reel
- HDMI & Deep Color are trademarks of Silicon Image

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