

## Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <http://www.nxp.com>, <http://www.philips.com/> or <http://www.semiconductors.philips.com/>, use <http://www.nexperia.com>

Instead of [sales.addresses@www.nxp.com](mailto:sales.addresses@www.nxp.com) or [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com), use [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com) (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

- © **Nexperia B.V. (year). All rights reserved.**

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

# 74HC4094-Q100; 74HCT4094-Q100

## 8-stage shift-and-store bus register

Rev. 1 — 30 January 2013

Product data sheet

### 1. General description

---

The 74HC4094-Q100; 74HCT4094-Q100 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (D) and two serial outputs (QS1 and QS2) to enable cascading. Data is shifted on the LOW-to-HIGH transitions of the CP input. Data is available at QS1 on the LOW-to-HIGH transitions of the CP input to allow cascading when clock edges are fast. The same data is available at QS2 on the next HIGH-to-LOW transition of the CP input to allow cascading when clock edges are slow. The data in the shift register is transferred to the storage register when the STR input is HIGH. Data in the storage register appears at the outputs whenever the output enable input (OE) is HIGH. A LOW on OE causes the outputs to assume a high-impedance OFF-state. Operation of the OE input does not affect the state of the registers. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

### 2. Features and benefits

---

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD7A
- Input levels:
  - ◆ For 74HC4094-Q100: CMOS level
  - ◆ For 74HCT4094-Q100: TTL level
- Low-power dissipation
- ESD protection:
  - ◆ MIL-STD-883, method 3015 exceeds 2000 V
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0  $\Omega$ )

### 3. Applications

---

- Serial-to-parallel data conversion
- Remote control holding register



## 4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC4094D-Q100 74HCT4094D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4094DB-Q100 74HCT4094DB-Q100	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC4094PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

## 5. Functional diagram

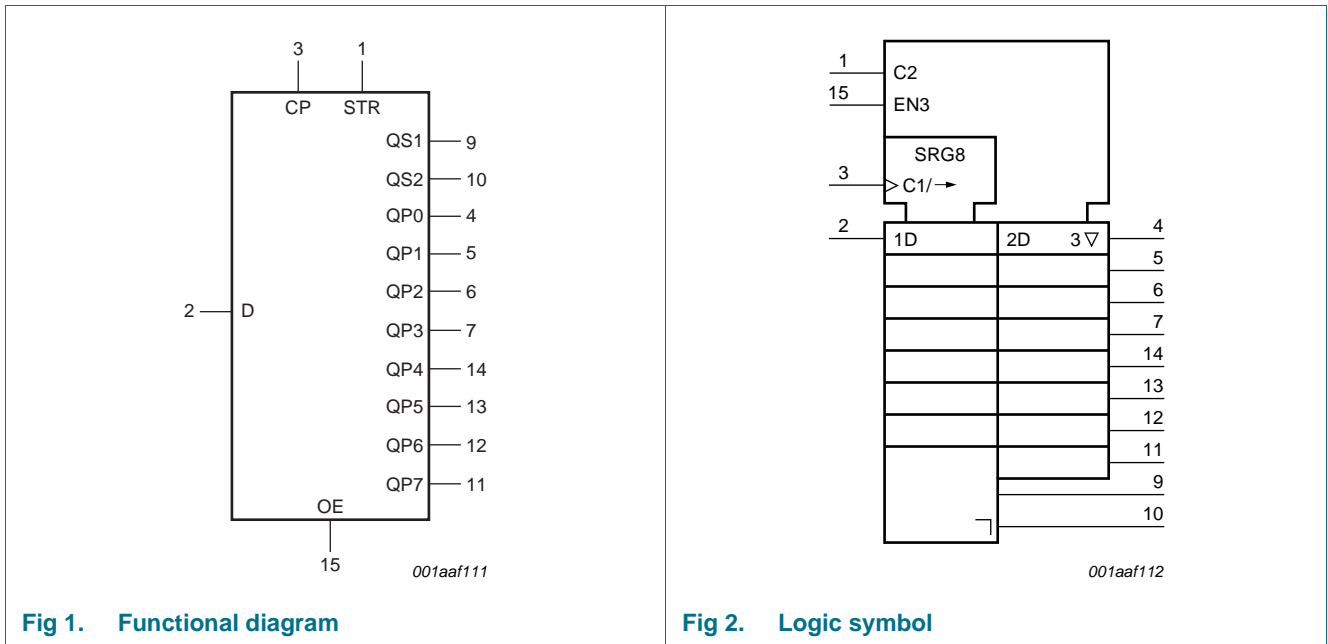


Fig 1. Functional diagram

Fig 2. Logic symbol

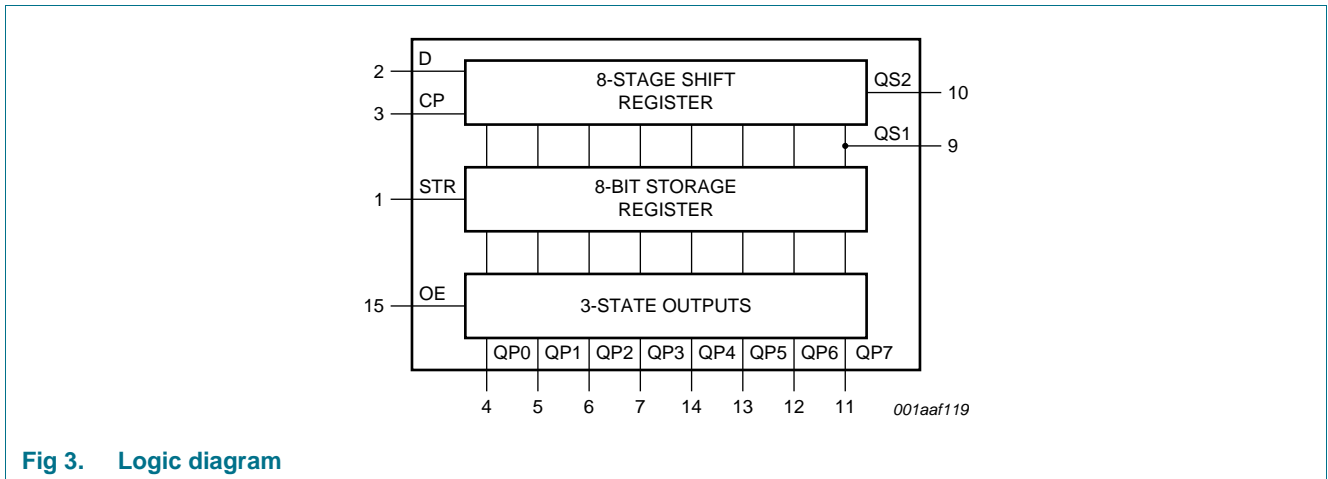


Fig 3. Logic diagram

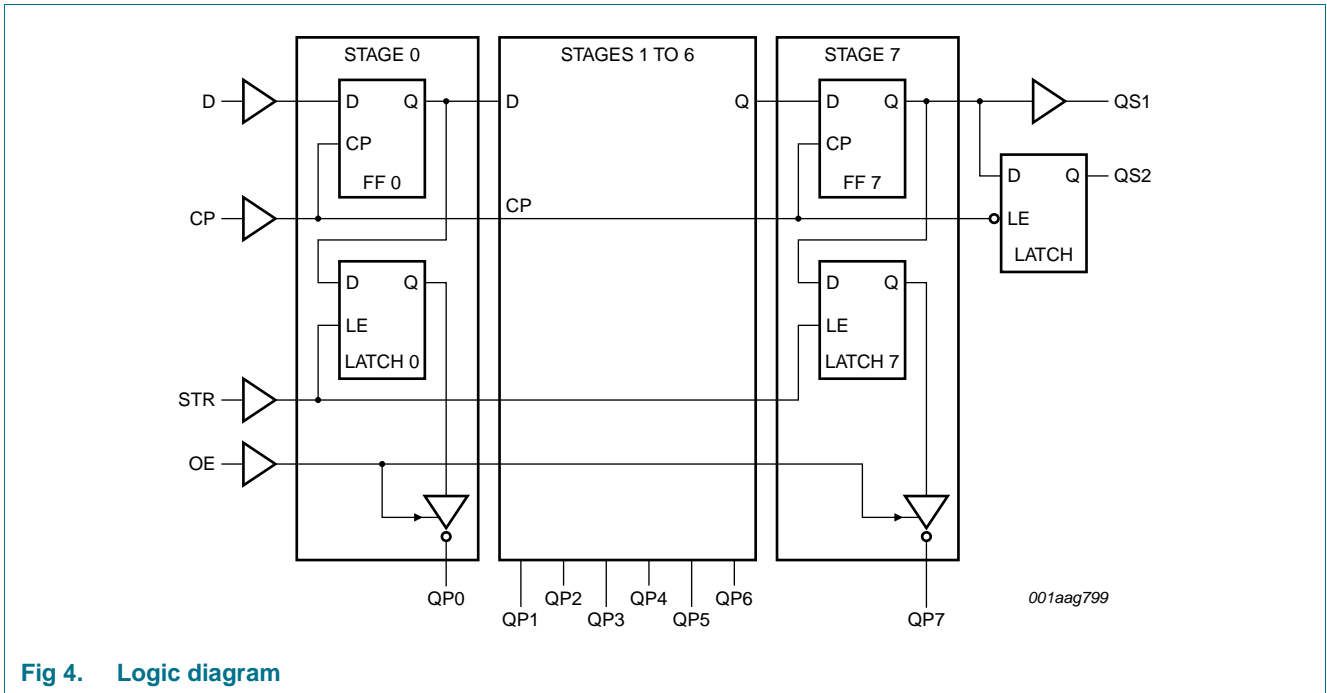


Fig 4. Logic diagram

## 6. Pinning information

### 6.1 Pinning

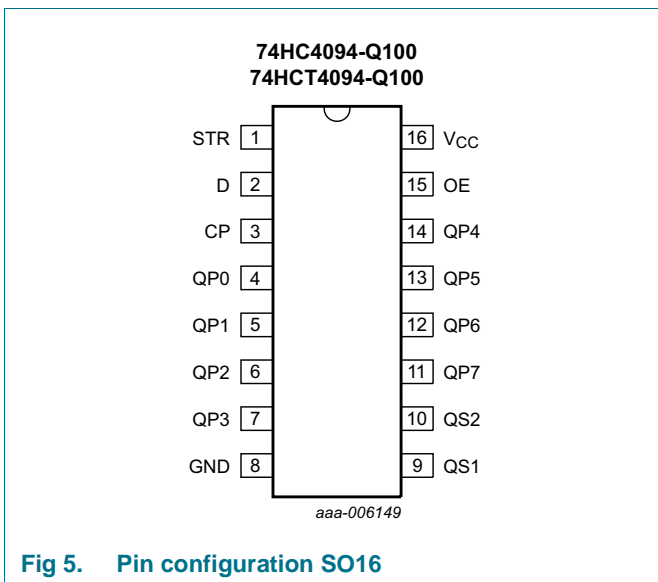


Fig 5. Pin configuration SO16

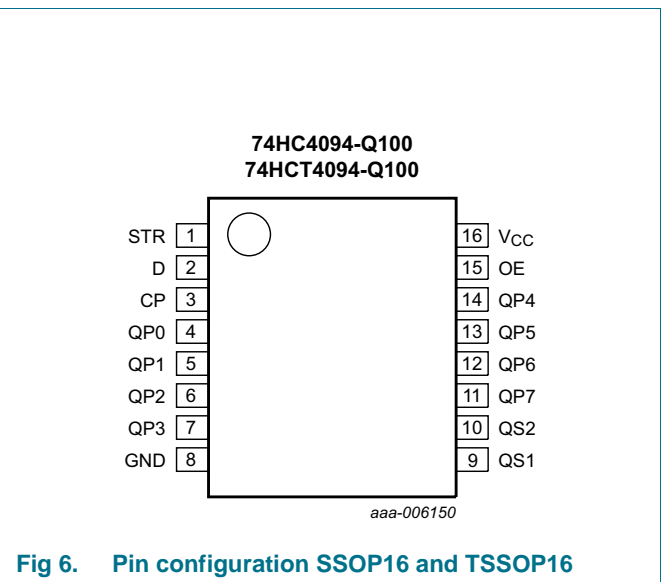


Fig 6. Pin configuration SSOP16 and TSSOP16

## 6.2 Pin description

**Table 2. Pin description**

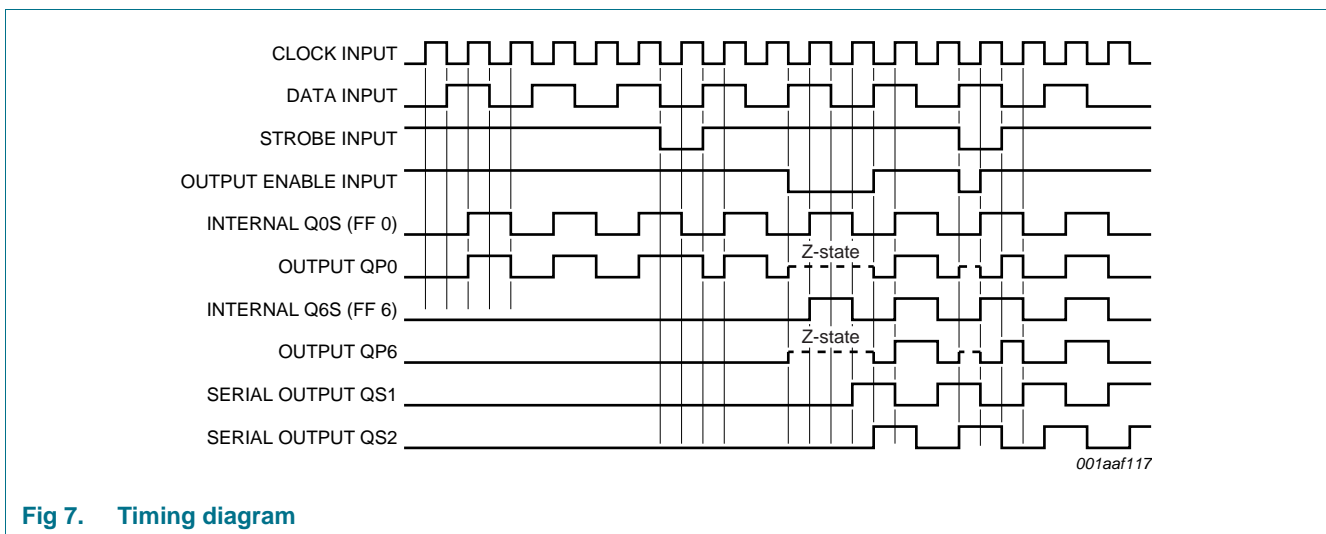
Symbol	Pin	Description
STR	1	strobe input
D	2	data input
CP	3	clock input
QP0 to QP7	4, 5, 6, 7, 14, 13, 12, 11	parallel output
V <sub>SS</sub>	8	ground supply voltage
QS1, QS2	9, 10	serial output
OE	15	output enable input
V <sub>DD</sub>	16	supply voltage

## 7. Functional description

**Table 3. Function table<sup>[1]</sup>**

Inputs				Parallel outputs		Serial outputs	
CP	OE	STR	D	QP0	QPn	QS1	QS2
↑	L	X	X	Z	Z	Q6S	NC
↓	L	X	X	Z	Z	NC	Q7S
↑	H	L	X	NC	NC	Q6S	NC
↑	H	H	L	L	QPn - 1	Q6S	NC
↑	H	H	H	H	QPn - 1	Q6S	NC
↓	H	H	H	NC	NC	NC	Q7S

- [1] At the positive clock edge, the information in the 7<sup>th</sup> register stage is transferred to the 8<sup>th</sup> register stage and the QSn outputs.  
 H = HIGH voltage level; L = LOW voltage level; X = don't care;  
 ↑ = positive-going transition; ↓ = negative-going transition;  
 Z = HIGH-impedance OFF-state; NC = no change;  
 Q6S = the data in register stage 6 before the LOW to HIGH clock transition;  
 Q7S = the data in register stage 7 before the HIGH to LOW clock transition.



**Fig 7. Timing diagram**

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	+50	mA
$I_{GND}$	ground current		-	-50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation		[1] -	500	mW

[1] For SO16:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

For SSOP16 and TSSOP16 packages:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC4094-Q100			74HCT4094-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

## 10. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit					
			Min	Typ	Max	Min	Max	Min	Max						
<b>74HC4094-Q100</b>															
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V					
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V					
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V					
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V					
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V					
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V					
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>													
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V					
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V					
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V					
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V					
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>													
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V					
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V					
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V					
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V					
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA					
		I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.5	-	±5.0	-	±10.0	μA			
				I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	-	80	-	160	μA	
						C <sub>I</sub>	input capacitance		-	3.5	-				pF
<b>74HCT4094-Q100</b>															
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V					
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V					
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V													
		I <sub>O</sub> = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V					
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V													
		I <sub>O</sub> = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V					
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V													
		I <sub>O</sub> = 20 μA	-	0	0.1	-	0.1	-	0.1	V					
		I <sub>O</sub> = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V					

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.1	-	±1.0	-	±1.0	µA
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND per input pin; other inputs at $V_{CC}$ or GND; $I_O = 0$ A	-	-	±0.5	-	±5.0	-	±10	µA
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	-	80	-	160	µA
$\Delta I_{CC}$	additional supply current	$V_I = V_{CC} - 2.1$ V; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A								
		per input pin; STR input	-	100	360	-	450	-	490	µA
		per input pin; OE input	-	150	540	-	675	-	735	µA
		per input pin; CP input	-	150	540	-	675	-	735	µA
		per input pin; D input	-	40	144	-	180	-	196	µA
$C_I$	input capacitance		-	3.5	-				pF	



## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC4094-Q100</b>										
$t_{pd}$	propagation delay	CP to QS1; see <a href="#">Figure 8</a> <sup>[1]</sup>								
		$V_{CC} = 2.0$ V	-	50	150	-	190	-	225	ns
		$V_{CC} = 4.5$ V	-	18	30	-	38	-	45	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	15	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	14	26	-	33	-	38	ns
		CP to QS2; see <a href="#">Figure 8</a> <sup>[1]</sup>								
		$V_{CC} = 2.0$ V	-	44	135	-	170	-	205	ns
		$V_{CC} = 4.5$ V	-	16	27	-	34	-	41	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	13	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	13	23	-	29	-	35	ns
		CP to QPn; see <a href="#">Figure 8</a> <sup>[1]</sup>								
		$V_{CC} = 2.0$ V	-	63	195	-	245	-	295	ns
		$V_{CC} = 4.5$ V	-	23	39	-	49	-	59	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	20	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	18	33	-	42	-	50	ns
		STR to QPn; see <a href="#">Figure 9</a> <sup>[1]</sup>								
$V_{CC} = 2.0$ V	-	58	180	-	225	-	270	ns		
$V_{CC} = 4.5$ V	-	21	36	-	45	-	54	ns		
$V_{CC} = 5$ V; $C_L = 15$ pF	-	18	-	-	-	-	-	ns		
$V_{CC} = 6.0$ V	-	17	31	-	38	-	46	ns		
$t_{en}$	enable time	OE to QPn; see <a href="#">Figure 11</a> <sup>[2]</sup>								
		$V_{CC} = 2.0$ V	-	55	175	-	220	-	265	ns
		$V_{CC} = 4.5$ V	-	20	35	-	44	-	53	ns
		$V_{CC} = 6.0$ V	-	16	30	-	37	-	45	ns
$t_{dis}$	disable time	OE to QPn; see <a href="#">Figure 11</a> <sup>[3]</sup>								
		$V_{CC} = 2.0$ V	-	41	125	-	155	-	190	ns
		$V_{CC} = 4.5$ V	-	15	25	-	31	-	38	ns
		$V_{CC} = 6.0$ V	-	12	21	-	26	-	32	ns
$t_t$	transition time	QPn and QSn; see <a href="#">Figure 8</a> <sup>[4]</sup>								
		$V_{CC} = 2.0$ V	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0$ V	-	6	13	-	16	-	19	ns

**Table 7. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$t_W$	pulse width	CP HIGH or LOW; see <a href="#">Figure 8</a>								
		$V_{CC} = 2.0$ V	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	5	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	4	-	17	-	20	-	ns
		STR HIGH; see <a href="#">Figure 9</a>								
		$V_{CC} = 2.0$ V	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	5	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	4	-	17	-	20	-	ns
		$t_{SU}$	set-up time	D to CP; see <a href="#">Figure 10</a>						
$V_{CC} = 2.0$ V	50			14	-	65	-	75	-	ns
$V_{CC} = 4.5$ V	10			5	-	13	-	15	-	ns
$V_{CC} = 6.0$ V	9			4	-	11	-	13	-	ns
CP to STR; see <a href="#">Figure 9</a>										
$V_{CC} = 2.0$ V	100			28	-	125	-	150	-	ns
$V_{CC} = 4.5$ V	20			10	-	25	-	30	-	ns
$V_{CC} = 6.0$ V	17			8	-	21	-	26	-	ns
$t_H$	hold time			D to CP; see <a href="#">Figure 10</a>						
		$V_{CC} = 2.0$ V	3	-6	-	3	-	3	-	ns
		$V_{CC} = 4.5$ V	3	-2	-	3	-	3	-	ns
		$V_{CC} = 6.0$ V	3	-2	-	3	-	3	-	ns
		CP to STR; see <a href="#">Figure 9</a>								
		$V_{CC} = 2.0$ V	0	-14	-	0	-	0	-	ns
		$V_{CC} = 4.5$ V	0	-5	-	0	-	0	-	ns
		$V_{CC} = 6.0$ V	0	-4	-	0	-	0	-	ns
		$f_{max}$	maximum frequency	CP; see <a href="#">Figure 8</a>						
$V_{CC} = 2.0$ V	6.0			28	-	4.8	-	4.0	-	MHz
$V_{CC} = 4.5$ V	30			87	-	24	-	20	-	MHz
$V_{CC} = 5$ V; $C_L = 15$ pF	-			95	-	-	-	-	-	MHz
$V_{CC} = 6.0$ V	35			103	-	28	-	24	-	MHz
$C_{PD}$	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_I = \text{GND to } V_{CC}$	<a href="#">5</a>	-	83	-	-	-	-	pF

**Table 7. Dynamic characteristics ...continued**

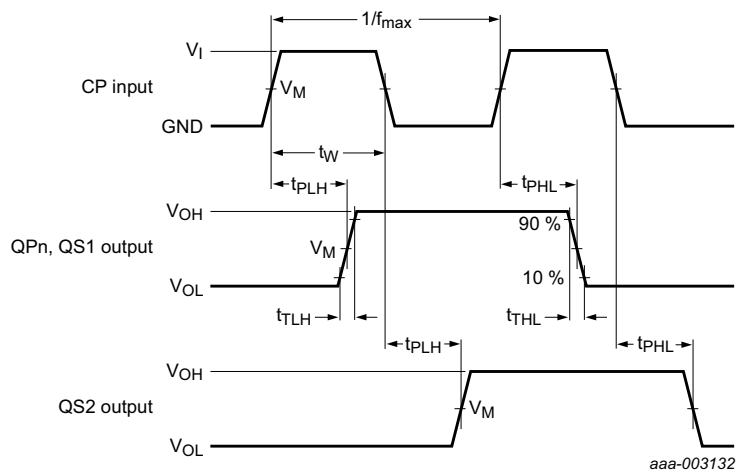
Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HCT4094-Q100</b>										
$t_{pd}$	propagation delay	CP to QS1; see <a href="#">Figure 8</a> <sup>[1]</sup>								
		$V_{CC} = 4.5$ V	-	23	39	-	49	-	59	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	19	-	-	-	-	-	ns
		CP to QS2; see <a href="#">Figure 8</a> <sup>[1]</sup>								
		$V_{CC} = 4.5$ V	-	21	36	-	45	-	54	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	18	-	-	-	-	-	ns
		CP to QPn; see <a href="#">Figure 8</a> <sup>[1]</sup>								
		$V_{CC} = 4.5$ V	-	25	43	-	54	-	65	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	21	-	-	-	-	-	ns
$t_{en}$	enable time	STR to QPn; see <a href="#">Figure 9</a> <sup>[1]</sup>								
		$V_{CC} = 4.5$ V	-	22	39	-	49	-	59	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	19	-	-	-	-	-	ns
$t_{dis}$	disable time	OE to QPn; see <a href="#">Figure 11</a> <sup>[3]</sup>								
		$V_{CC} = 4.5$ V	-	21	35	-	44	-	53	ns
$t_t$	transition time	OE to QPn; see <a href="#">Figure 11</a> <sup>[3]</sup>								
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
$t_W$	pulse width	QFn and QSn; see <a href="#">Figure 8</a> <sup>[4]</sup>								
		CP HIGH or LOW; see <a href="#">Figure 8</a>								
		$V_{CC} = 4.5$ V	16	7	-	20	-	24	-	ns
$t_{su}$	set-up time	STR HIGH; see <a href="#">Figure 9</a>								
		$V_{CC} = 4.5$ V	16	5	-	20	-	24	-	ns
$t_{su}$	set-up time	Dn to CP; see <a href="#">Figure 10</a>								
		$V_{CC} = 4.5$ V	10	4	-	13	-	15	-	ns
		CP to STR; see <a href="#">Figure 9</a>								
$t_h$	hold time	$V_{CC} = 4.5$ V	20	9	-	25	-	30	-	ns
		Dn to CP; see <a href="#">Figure 10</a>								
		$V_{CC} = 4.5$ V	4	0	-	4	-	4	-	ns
$f_{max}$	maximum frequency	CP to STR; see <a href="#">Figure 9</a>								
		$V_{CC} = 4.5$ V	0	-4	-	0	-	0	-	ns
		CP; see <a href="#">Figure 8</a>								
$C_{PD}$	power dissipation capacitance	$V_{CC} = 4.5$ V	30	80	-	24	-	20	-	MHz
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	86	-	-	-	-	-	MHz
		$C_L = 50$ pF; $f = 1$ MHz; $V_I = GND$ to $V_{CC}$ <sup>[5]</sup>	-	92	-	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

- [2]  $t_{en}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .
- [3]  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .
- [4]  $t_i$  is the same as  $t_{THL}$  and  $t_{TLH}$ .
- [5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in V;  
 $N$  = number of inputs switching;  
 $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

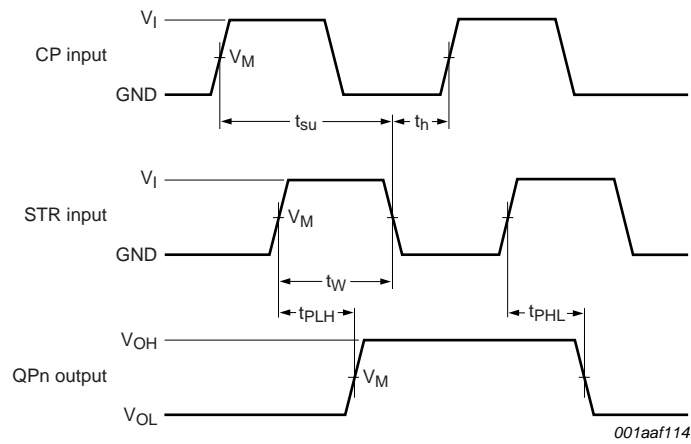
## 12. Waveforms



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

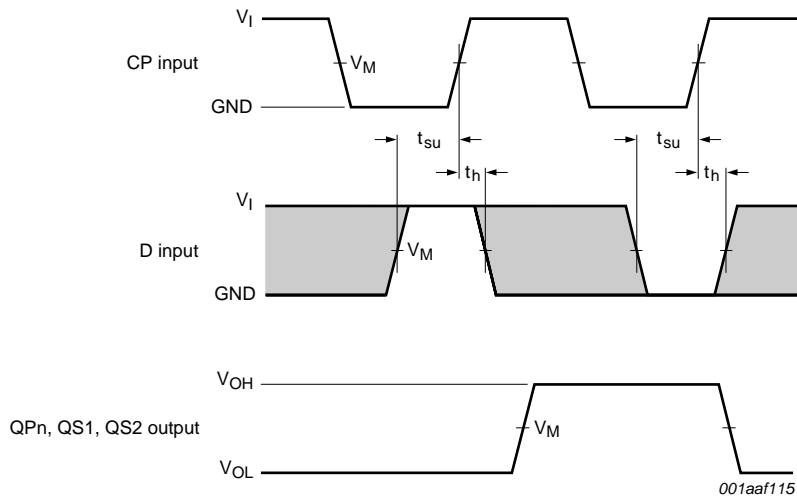
**Fig 8. Propagation delay input (CP) to output (QPn, QS1, QS2), output transition time, clock input (CP) pulse width and the maximum frequency (CP)**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

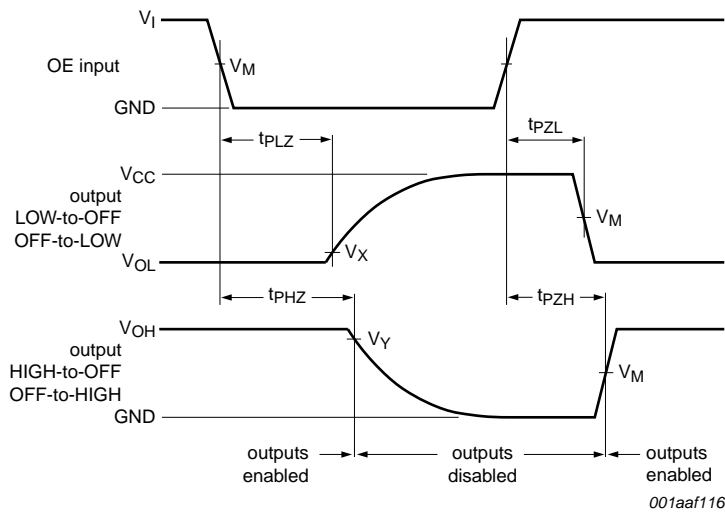
**Fig 9. Propagation delay strobe input (STR) to output (QPn), strobe input (STR) pulse width and the clock set-up and hold times for strobe input**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 10. The data input (D) to clock input (CP) set-up times and clock input (CP) to data input (D) hold times**

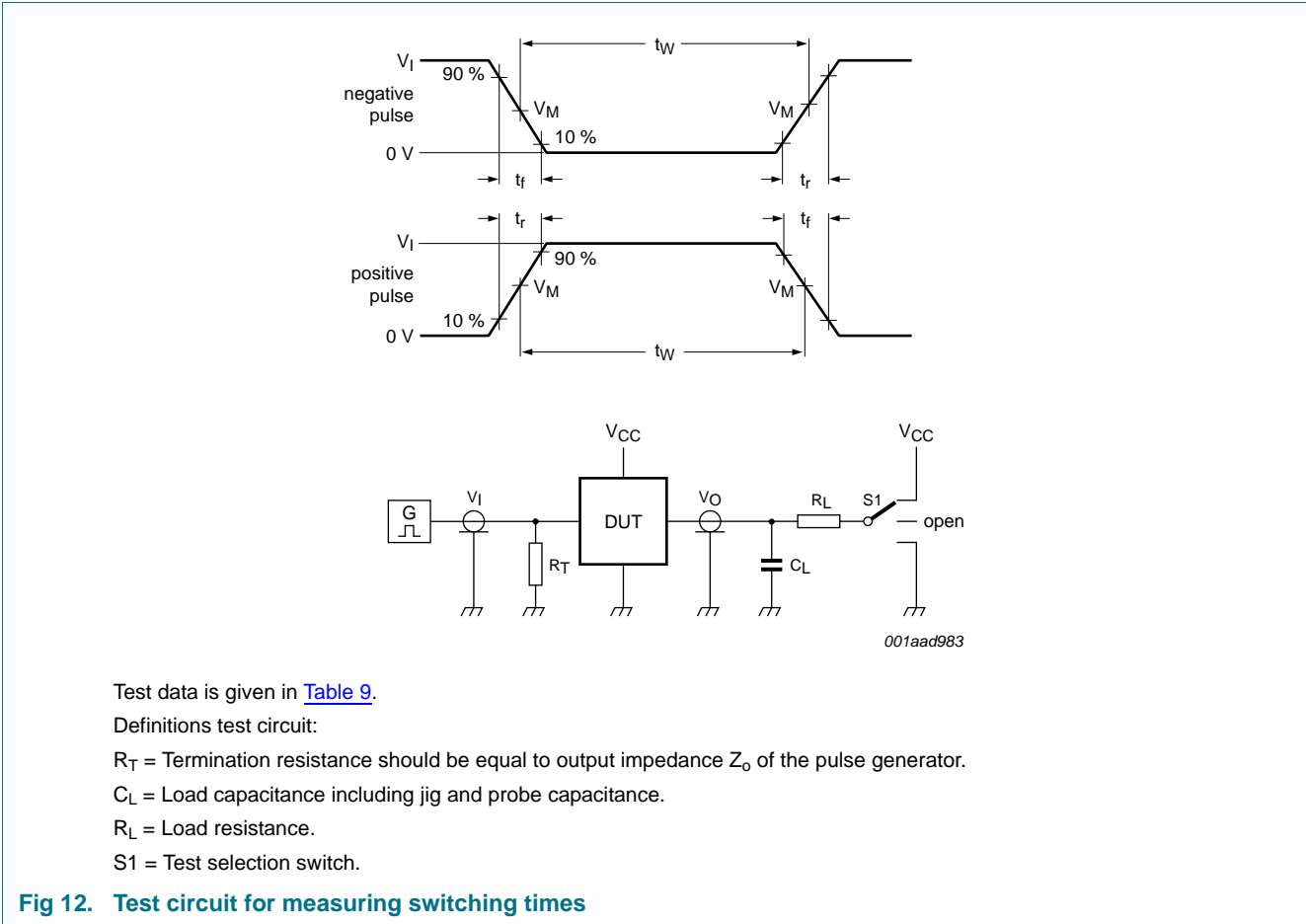


Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 11. Enable and disable times**

**Table 8. Measurement points**

Type	Input	Output		
	$V_M$	$V_M$	$V_X$	$V_Y$
74HC4094-Q100	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{OH}$	$0.9V_{OH}$
74HCT4094-Q100	1.3 V	1.3 V	$0.1V_{OH}$	$0.9V_{OH}$



**Table 9. Test data**

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74HC4094-Q100	$V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74HCT4094-Q100	3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

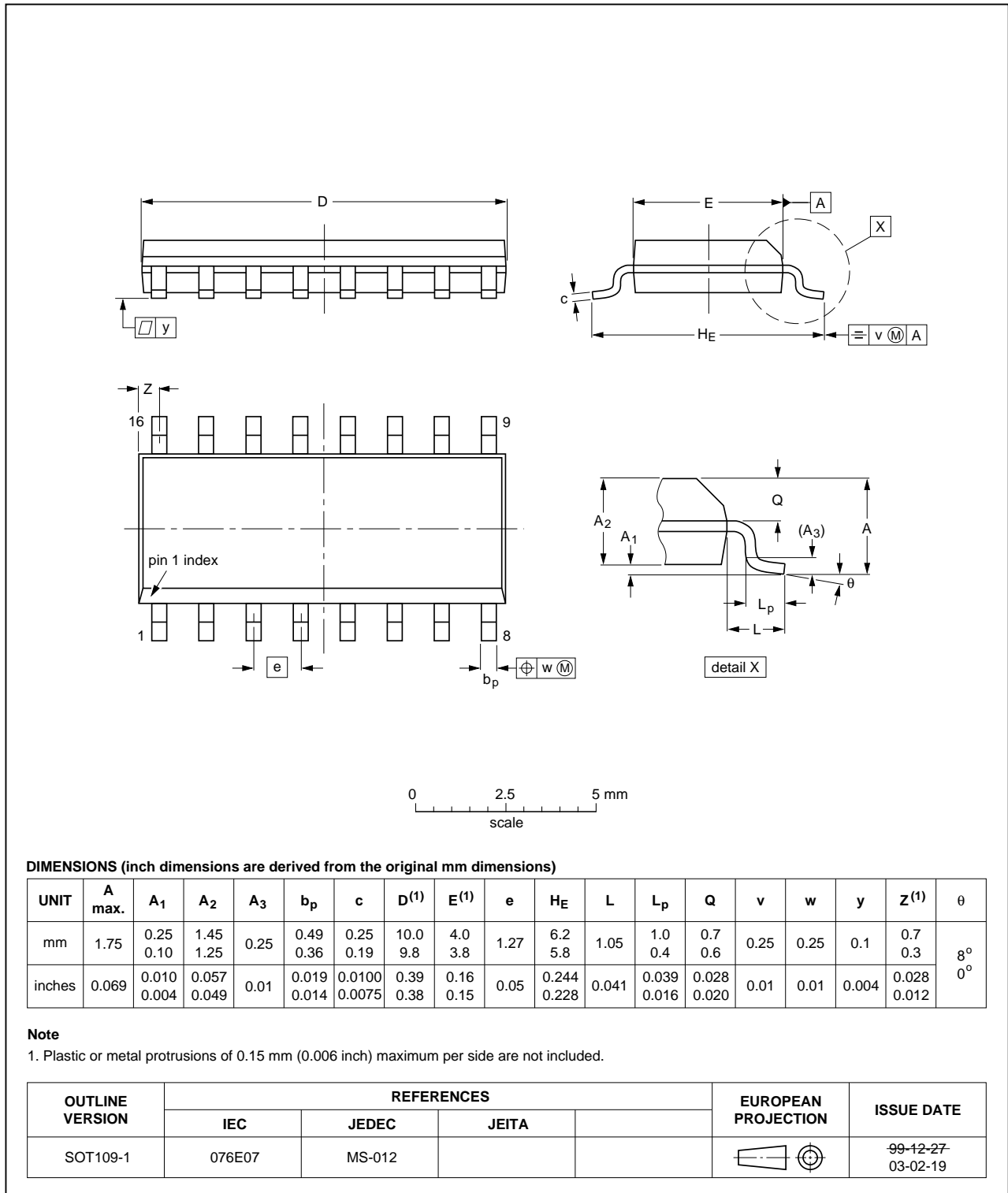


Fig 13. Package outline SOT109-1 (SO16)



SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

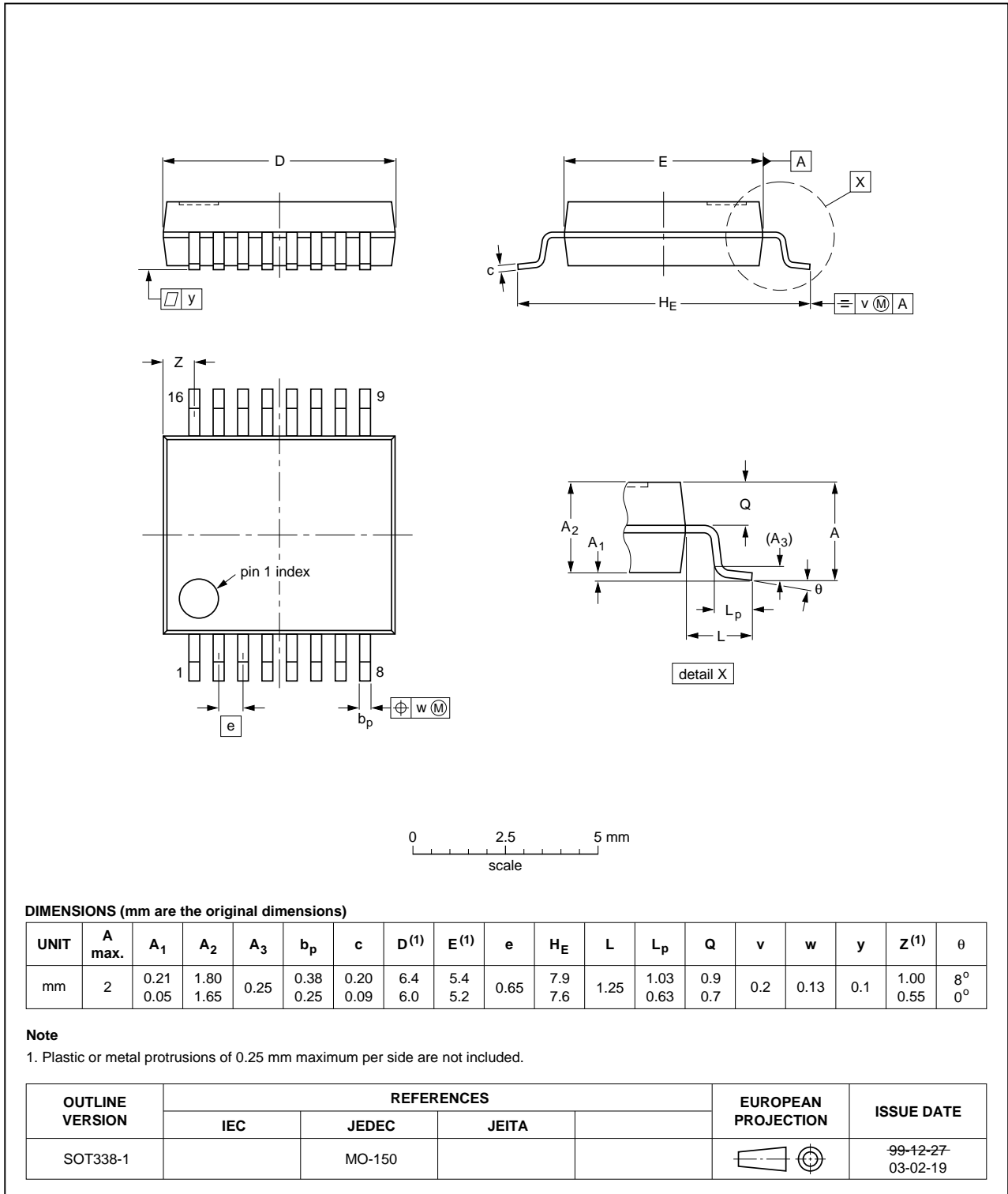


Fig 14. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

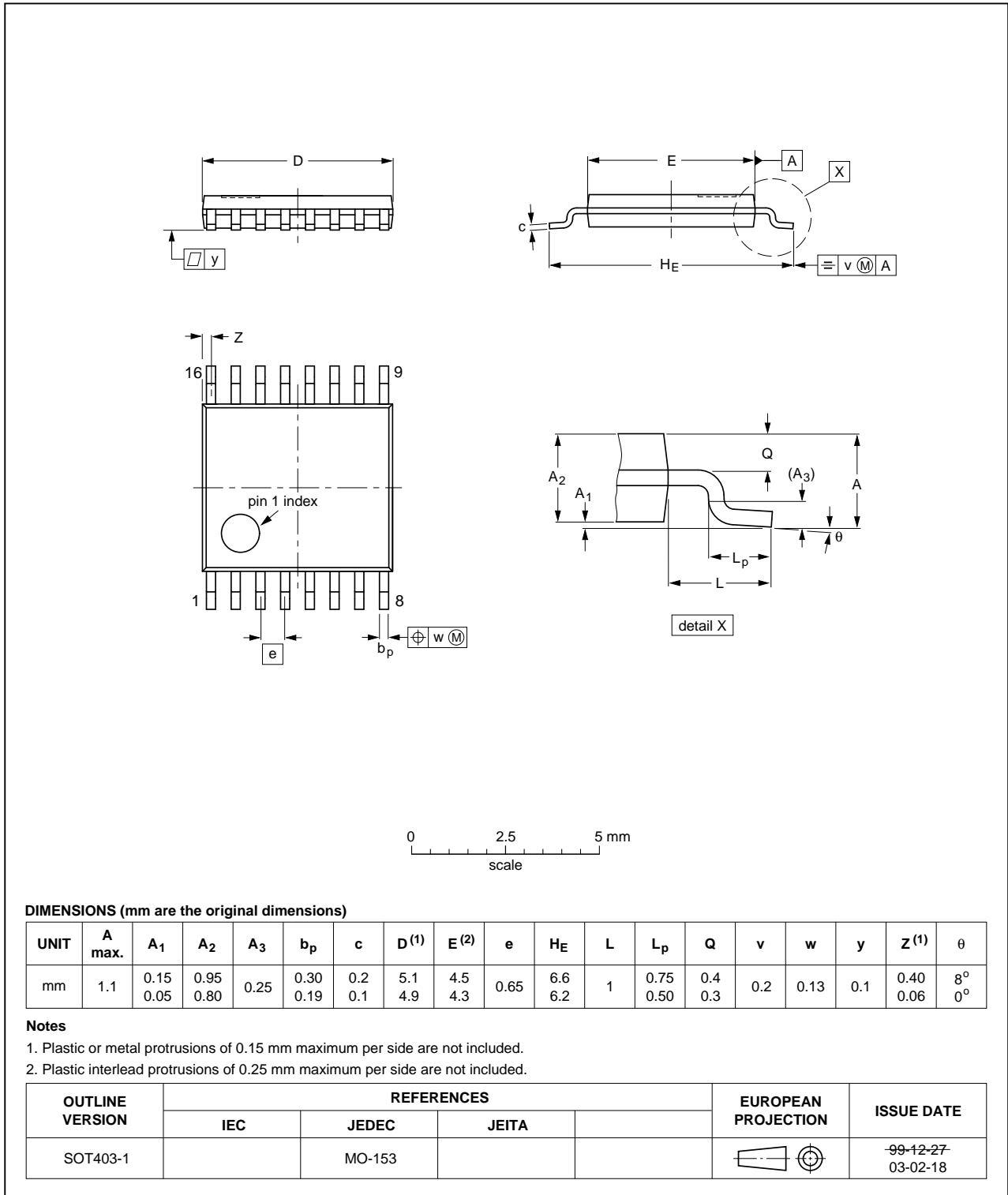


Fig 15. Package outline SOT403-1 (TSSOP16)

## 14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
MIL	Military

## 15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4094_Q100 v.1	20130130	Product data sheet	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 16.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 16.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use in automotive applications** — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 17. Contact information

---

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 18. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Applications</b> .....	<b>1</b>
<b>4</b>	<b>Ordering information</b> .....	<b>2</b>
<b>5</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>6</b>	<b>Pinning information</b> .....	<b>3</b>
6.1	Pinning .....	3
6.2	Pin description .....	4
<b>7</b>	<b>Functional description</b> .....	<b>4</b>
<b>8</b>	<b>Limiting values</b> .....	<b>5</b>
<b>9</b>	<b>Recommended operating conditions</b> .....	<b>5</b>
<b>10</b>	<b>Static characteristics</b> .....	<b>6</b>
<b>11</b>	<b>Dynamic characteristics</b> .....	<b>8</b>
<b>12</b>	<b>Waveforms</b> .....	<b>11</b>
<b>13</b>	<b>Package outline</b> .....	<b>15</b>
<b>14</b>	<b>Abbreviations</b> .....	<b>18</b>
<b>15</b>	<b>Revision history</b> .....	<b>18</b>
<b>16</b>	<b>Legal information</b> .....	<b>19</b>
16.1	Data sheet status .....	19
16.2	Definitions .....	19
16.3	Disclaimers .....	19
16.4	Trademarks .....	20
<b>17</b>	<b>Contact information</b> .....	<b>20</b>
<b>18</b>	<b>Contents</b> .....	<b>21</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2013.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 30 January 2013

Document identifier: 74HC\_HCT4094\_Q100