FemtoClock® Crystal/LVCMOS-to-3.3V LVPECL Frequency Synthesizer

843004I-04

DATASHEET

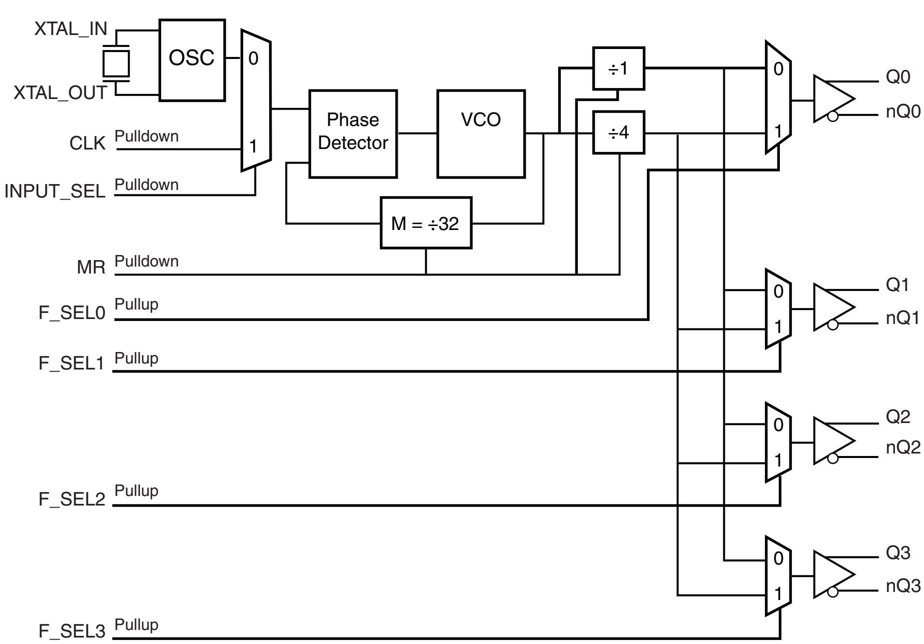
General Description

The 843004I-04 is a 4 output LVPECL Synthesizer optimized to generate clock frequencies for a variety of high performance applications. This device can select its input reference clock from either a crystal input or a single-ended clock signal. It can be configured to generate 4 outputs with individually selectable divide-by-one or divide-by-four function via the 4 frequency select pins (F_SEL[3:0]). The 843004I-04 uses IDT's 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter. This ensures that it will easily meet clocking requirements for SDH (STM-1/STM-4/STM-16) and SONET (OC-3/OC12/OC-48). This device is suitable for multi-rate and multiple port line card applications. The 843004I-04 is conveniently packaged in a small 24-pin TSSOP package.

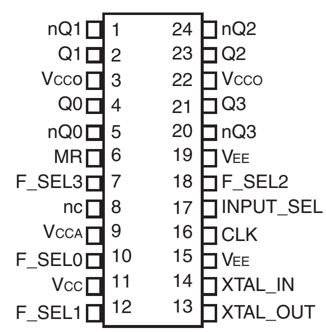
Features

- Four LVPECL outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Supports the following applications: SONET/SDH, SATA, or 10Gb Ethernet
- Output frequency range: 140MHz - 170MHz, 560MHz - 680MHz
- VCO range: 560MHz - 680MHz
- Crystal oscillator and CLK range: 17.5MHz - 21.25MHz
- RMS phase jitter @ 622.08MHz output, using a 19.44MHz crystal (12kHz - 20MHz): 0.82ps (typical)
- RMS phase jitter @ 156.25MHz output, using a 19.53125MHz crystal (1.875MHz - 20MHz): 0.57ps (typical)
- RMS phase jitter @ 155.52MHz output, using a 19.44MHz crystal (12kHz - 20MHz): 0.94ps (typical)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free RoHS compliant package

Block Diagram



Pin Assignment



843004I-04
24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
3, 22	V_{CCO}	Power		Output supply pins.
4, 5	Q0, nQ0	Ouput		Differential output pair. LVPECL interface levels.
6	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
7, 10, 12, 18	F_SEL3, F_SEL0, F_SEL1, F_SEL2	Input	Pullup	Frequency select pins. LVCMOS/LVTTL interface levels. See Table 3.
8	nc	Unused		No connect.
9	V_{CCA}	Power		Analog supply pin.
11	V_{CC}	Power		Core supply pin.
13, 14	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
15, 19	V_{EE}	Power		Negative supply pins.
16	CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
17	INPUT_SEL	Input	Pulldown	Selects between crystal or CLK inputs as the the PLL Reference source. Selects XTAL inputs when LOW. Selects CLK when HIGH. LVCMOS/LVTTL interface levels.
20, 21	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
23, 24	Q2, nQ2	Output		Differential output pair. LVPECL interface levels.

NOTE: refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Table 3. Output Configuration and Frequency Range Function Table

Inputs		VCO (MHz)	Divider Value	Output Frequency (MHz)	Application
F_SELx	XTAL (MHz)			Q0/nQ0:Q3/nQ3	
0	19.44	622.08	÷1	622.08	SONET/SDH
1	19.44	622.08	÷4	155.52	
0	18.75	600	÷1	600	SATA
1	18.75	600	÷4	150	
0	19.53125	625	÷1	625	10 Gigabit Ethernet
1	19.53125	625	÷4	156.25	
0	20.141601	644.5312	÷1	644.5312	10 Gigabit Ethernet 66B/64B FEC
1	20.141601	644.5312	÷4	161.13	

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	70°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				120	mA
I_{CCA}	Analog Supply Current				10	mA
I_{CCO}	Output Supply Current				120	mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK, MR, INPUT_SEL	$V_{CC} = V_{IN}$ = 3.465			150	µA
I_{IH}	Input High Current	F_SEL0:F_SEL3	$V_{CC} = V_{IN}$ = 3.465			5	µA
I_{IL}	Input Low Current	CLK, MR, INPUT_SEL	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
I_{IL}	Input Low Current	F_SEL0:F_SEL3	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. LVPECL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50 to V_{CCO} - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		17.5		21.25	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

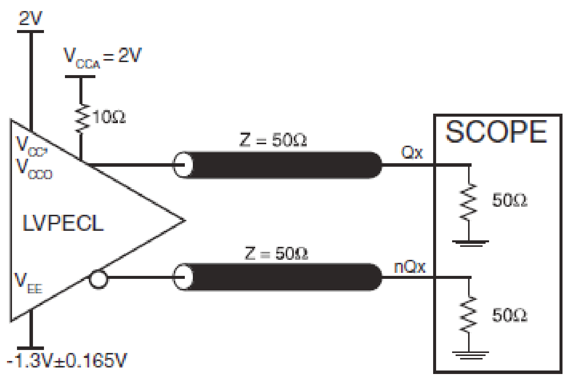
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = -40°C TO 85°C

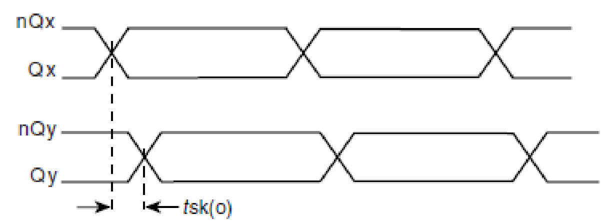
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Output Divider = ÷1	560		680	MHz
		Output Divider = ÷4	140		170	MHz
tsk(o)	Output Skew; NOTE 1, 2, 3				75	ps
tjit(Ø)	RMS Phase Jitter (Random); NOTE 4	155.52MHz, Integration Range: 12kHz - 20MHz		0.94		ps
		156.25MHz, Integration Range: 1.875MHz - 20MHz		0.57		ps
		622.08MHz, Integration Range: 12kHz - 20MHz		82		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	175		675	ps
odc	Output Duty Cycle	Output Divider = ÷4	48		52	%
		Output Divider = ÷1	40		60	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at V_{CCO}/2.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Output skew measurements taken with all outputs in the same divide configuration.
NOTE 4: Please refer to the Phase Noise Plot.

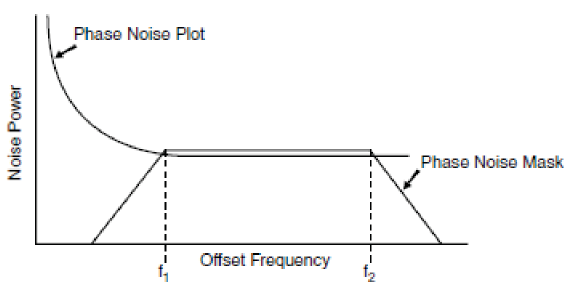
Parameter Measurement Information



3.3V Core/3.3V Output Load AC Test Circuit

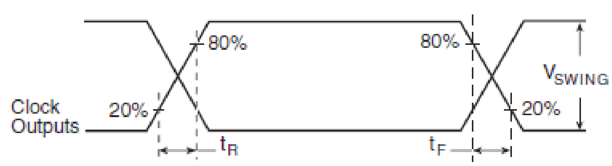


Output Skew

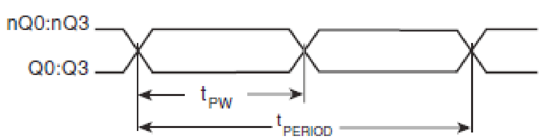


$$\text{RMS Jitter} = \sqrt{\text{Area Under the Masked Phase Noise Plot}}$$

RMS Phase Jitter



Output Rise/Fall Time



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/Period

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 843004I-04 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10μF and a .01μF bypass capacitor should be connected to each V_{CCA}.

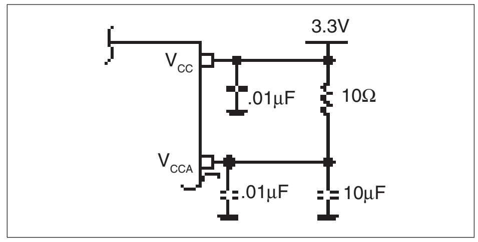


Figure 1. Power Supply Filtering

Crystal Input Interface

The 843004I-04 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 19.44MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

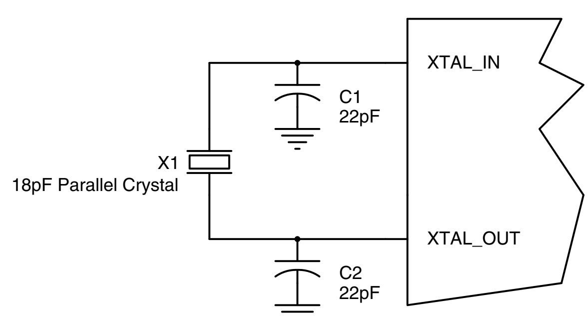


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

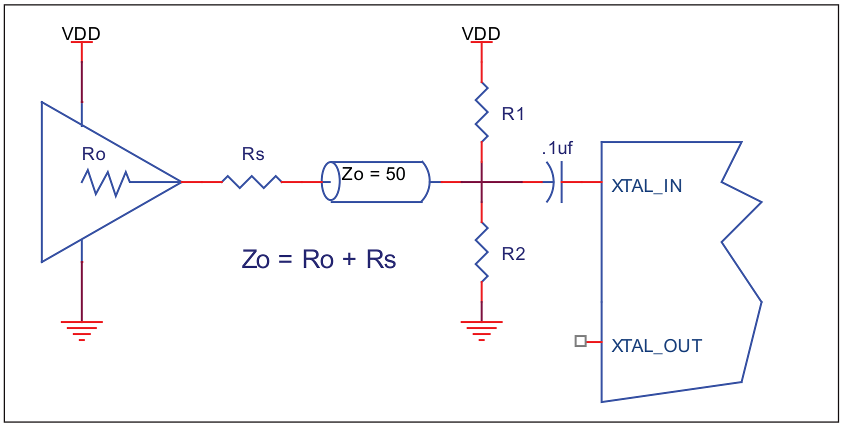


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Input:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK Input:
For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Output
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Output

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

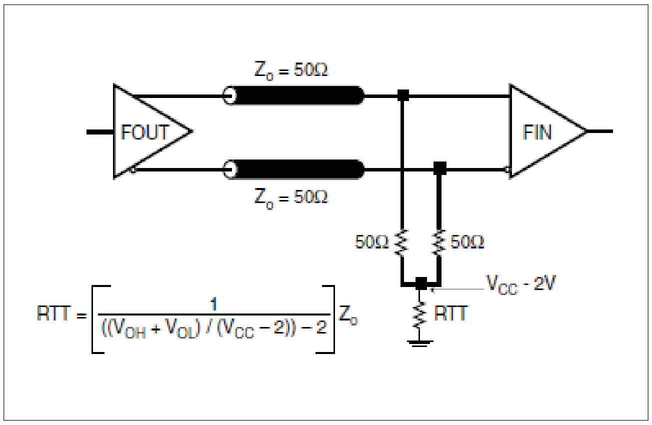


Figure 4A. LVPECL Output Termination

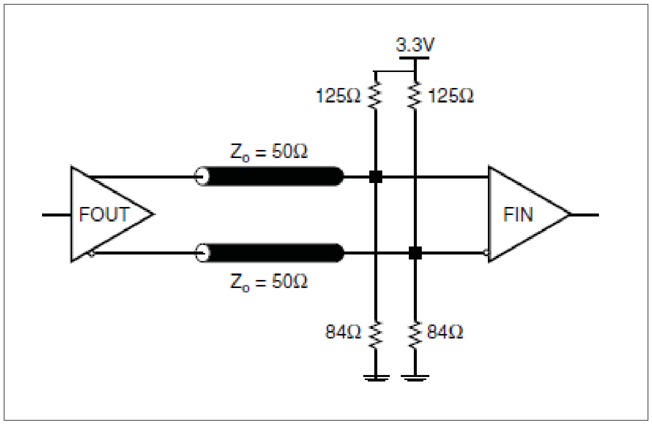


Figure 4B. LVPECL Output Termination

Schematic Example

Figure 5 shows a schematic example for 843004I-04. In this example, the input is a 19.44MHz parallel resonant crystal with load capacitor CL=18pF. The 22pF frequency fine tuning capacitors are used C1 and C2. This example also shows general logic control input handling. For decoupling capacitors, it is recommended to have one decouple capacitor per power pin. Each decoupling capacitor should be located as close as possible to the power pin. The low pass filter R2, C3 and C4 should also be located as close to the V_{CCA} pin as possible.

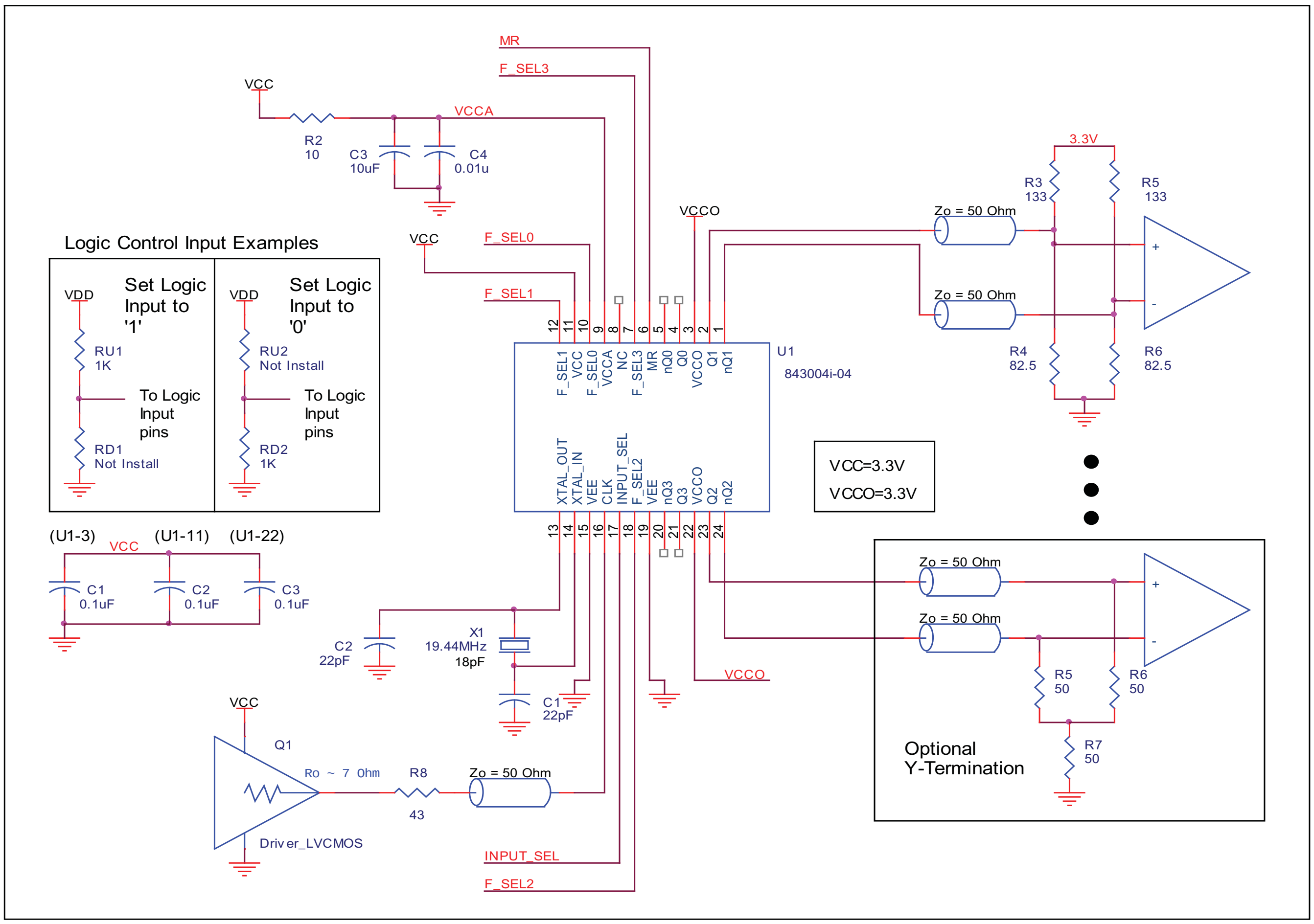


Figure 5. ICS844004I-04 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 843004I-04.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 843004I-04 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 120mA = **415.8mW**
- Power (outputs)$_{MAX}$ = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30mW = **120mW**

Total Power $_{\_MAX}$ (3.465V, with all outputs switching) = 415.8 + 120mW = **535.8mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A
Tj = Junction Temperature
θ_{JA} = Junction-to-Ambient Thermal Resistance
Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming an air flow of 1 meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.536W * 65°C/W = 119.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 7. Thermal Resistance θ_{JA} for 24-Lead TSSOP, Forced Convection

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in the *Figure 6.*

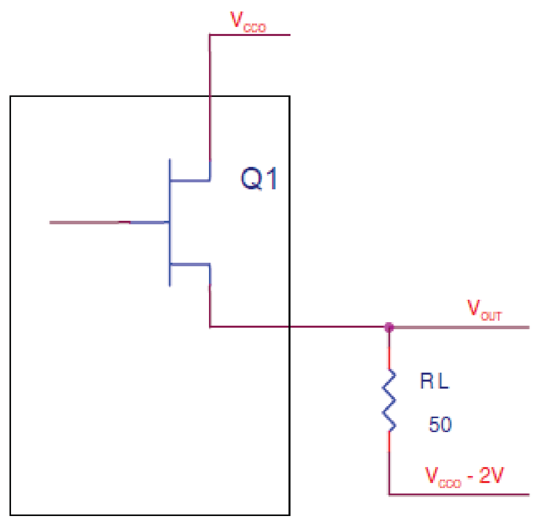


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$

$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$

$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 24 Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

Transistor Count

The transistor count for 843004I-04 is: 2273

Package Outline - G Suffix for 24 Lead TSSOP

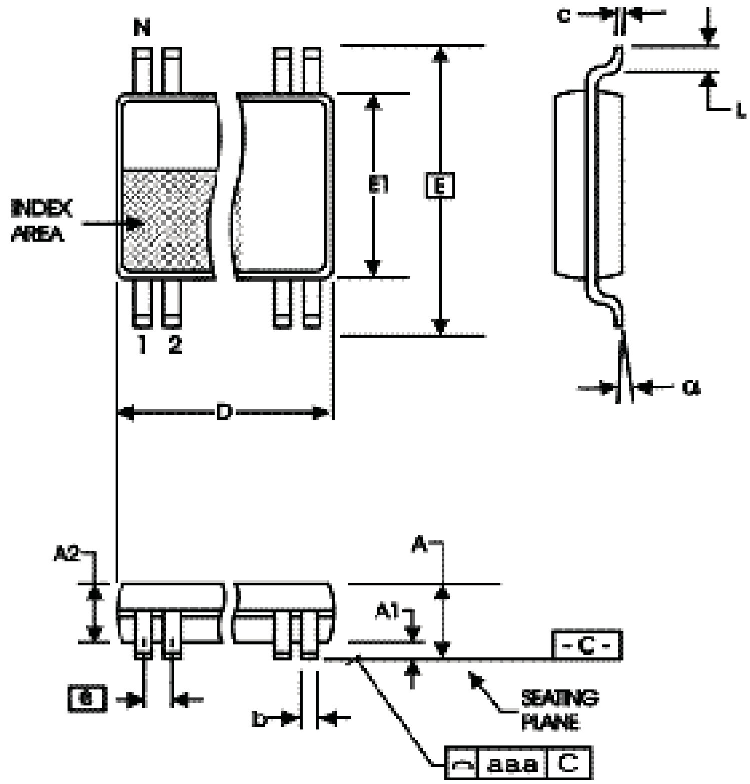


Table 9. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843004AGI-04LF	ICS43004AI04L	24 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
843004AGI-04LFT	ICS43004AI04L	24 Lead "Lead-Free" TSSOP	tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T10	14 16	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	7/26/10
A	T10	14	Updated data sheet format. Ordering Information - Removed leaded devices.	5/17/15

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