PIC18F2410/2510/4410/4510 Rev. B2 Silicon Errata

The PIC18F2410/2510/4410/4510 Rev. B2 parts you have received conform functionally to the Device Data Sheet (DS39636**D**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2410/2510/4410/4510 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F2410/2510/4410/4510 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2410	0001 0001 011	0 0101
PIC18F2510	0001 0001 001	0 0101
PIC18F4410	0001 0000 111	0 0101
PIC18F4510	0001 0000 101	0 0101

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: MSSP

In SPI Slave mode, with slave select enabled (SSPM<3:0> = 0100), the minimum time between the falling edge of the $\overline{SS}$ pin and first SCK edge is greater than specified in parameter 70 in Table 25-16 and Table 25-17. The updated specification is shown in bold in Table 1.

The minimum time between the $\overline{SS}$ pin low and an SSPBUF write is also 3 TCY. If the falling edge of the $\overline{SS}$ pin occurs greater than 3 TCY before the first SCK edge, or loading SSPBUF, the peripheral will function correctly. Also, if SSPBUF is written prior to the $\overline{SS}$ pin going low, the peripheral will function correctly.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

TABLE 1: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING)

Param No.	Symbol	Characteristic	Min.	Max.	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}$ ↓ to SCK ↓ or SCK ↑ Input	**3 TCY**	—	ns	

2. Module: MSSP

With MSSP in SPI Master mode, FOSC/64 or Timer2/2 clock rate, and CKE = 0, a write collision may occur if SSPBUF is loaded immediately after the transfer is complete. A delay may be required after the MSSP Interrupt Flag bit, SSPIF, is set or the Buffer Full bit, BF, is set and before writing SSPBUF. If the delay is insufficiently short, a write collision may occur, as indicated by the WCOL bit being set.

Work around

Add a software delay of one SCK period after detecting the completed transfer and prior to updating the SSPBUF contents. Verify the WCOL bit is clear after writing SSPBUF. If the WCOL is set, clear the bit in software and rewrite the SSPBUF register.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: Enhanced Capture/Compare/ PWM (ECCP)

With the ECCP configured for Half-Bridge PWM mode (CCP1M<3:0> = 1110), the output may be corrupted for particular duty cycle selections. Affected duty cycle values are 0 though 3, and every subsequent increment of 4 (i.e., 7, 11, 15, 19, etc.).

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: Timer1 and Timer3

When either Timer1 or Timer3 is configured to use the external clock source in 8-Bit Asynchronous mode (T1CON<7:0> or T3CON<7:0> = 0xxx x111), writes to the corresponding TMRxH:TMRxL registers may not occur as expected.

For the purposes of this issue, instructions that directly affect the contents of the Timer registers are considered to be writes. This includes CLRF, SETF and MOVF instructions.

Work around

Insert a delay of one instruction cycle between writes to TMRxH and TMRxL. This delay can be a NOP, or any instruction that does not access the Timer registers (Example 1).

EXAMPLE 1: ONE INSTRUCTION DELAY

```
CLRF    TMR1H
MOVLW   T1Offset  ; 1 Tcy delay
MOVWF   TMR1L
```

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: Timer1/3

When Timer1 or Timer3 is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur if an external clock edge arrives too soon following a firmware write to the TMRxH:TMRxL registers. An unexpected interrupt flag event may also occur when enabling the module or switching from Synchronous to Asynchronous mode.

Work around

This issue only applies when operating the timer in Asynchronous mode. Whenever possible, operate the timer module in Synchronous mode to avoid spurious timer interrupts.

If Asynchronous mode must be used in the application, potential strategies to mitigate the issue may include any of the following:

- Design the firmware so it does not rely on the TMRxIF flag or keep the respective interrupt disabled. The timer still counts normally and does not reset to `0x0000` when the spurious interrupt flag event is generated.
- Design the firmware so that it does not write to the TMRxH:TMRxL registers or does not periodically disable/enable the timer, or switch modes. Reading from the timer does not trigger the spurious interrupt flag events.
- If the firmware must use the timer interrupts and must write to the timer (or disable/enable, or mode switch the timer), implement code to suppress the spurious interrupt event, should it occur. This can be achieved by following the process shown in Example 2.

EXAMPLE 2: ASYNCHRONOUS TIMER MODE WORK AROUND TO AVOID SPURIOUS INTERRUPT

```
//Timer1 update procedure in asynchronous mode
//The code below uses Timer1 as example

T1CONbits.TMR1ON = 0;          //Stop timer from incrementing
PIE1bits.TMR1IE = 0;           //Temporarily disable Timer1 interrupt vectoring
TMR1H = 0x00;                  //Update timer value
TMR1L = 0x00;
T1CONbits.TMR1ON = 1;          //Turn on timer

//Now wait at least two full T1CKI periods + 2TCY before re-enabling Timer1 interrupts.
//Depending upon clock edge timing relative to TMR1H/TMR1L firmware write operation,
//a spurious TMR1IF flag event may sometimes assert. If this happens, to suppress
//the actual interrupt vectoring, the TMR1IE bit should be kept clear until
//after the "window of opportunity" (for the spurious interrupt flag event has passed).
//After the window is passed, no further spurious interrupts occur, at least
//until the next timer write (or mode switch/enable event).

while(TMR1L < 0x02);           //Wait for 2 timer increments more than the Updated Timer
                               //value (indicating more than 2 full T1CKI clock periods elapsed)
NOP();                         //Wait two more instruction cycles
NOP();
PIR1bits.TMR1IF = 0;           //Clear TMR1IF flag, in case it was spuriously set
PIE1bits.TMR1IE = 1;           //Now re-enable interrupt vectoring for timer 1
```

6. Module: Enhanced Universal Synchronous Receiver Transmitter (EUSART)

One bit has been added to the BAUDCON register and one bit has been renamed. The added bit is RXDTP and is in the location, BAUDCON<5>. The renamed bit is the TXCKP bit (BAUDCON<4>), which had been named SCKP.

The TXCKP (BAUDCON<4>) and RXDTP (BAUDCON<5>) bits enable the TX and RX signals to be inverted (polarity reversed).

Register 17-3, on page 194, will be changed as shown on page 3.

Work around

None required.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: 10-Bit Analog-to-Digital (A/D) Converter

When the A/D clock source is selected as 2 TOSC or RC (when ADCS2:ADCS0 = 000 or x11), in extremely rare cases, the EIL (Integral Linearity Error) and EDL (Differential Linearity Error) may exceed the data sheet specification at codes 511 and 512 only.

Work around

Select a different A/D clock source (4 TOSC, 8 TOSC, 16 TOSC, 32 TOSC, 64 TOSC) and avoid selecting the 2 TOSC or RC modes.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (10/2006)

First revision of this document. Silicon issues 1-2 (MSSP), 3 (ECCP) and 4 (Timer1 and Timer3).

Rev B Document (4/2007)

Added silicon issue 5 (Enhanced Universal Synchronous Receiver Transmitter – EUSART).

Rev C Document (8/2007)

Added silicon issue 6 (10-Bit A/D Converter).

Rev D Document (01/2015)

Added silicon issue 5 (Timer 1/3).

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