

## GENERAL DESCRIPTION

This document provides an overview and suggested lab test setups of the evaluation board for Analog Devices' new ADCMP572/ADCMP573/ADCMP580/ADCMP581/ADCMP582 comparator products. Because these comparators represent state of the art, general-purpose comparator technology, it is important that their performance characteristics be evaluated using the highest bandwidth components available. The evaluation board provides a relatively high quality environment in which to make such measurements. All five device types are fully released to production.

This document should be used in conjunction with the ADCMP57x/ADCMP58x data sheets that contain full technical details on the device specifications and operation. The same PCB is used to evaluate the ADCMP572, ADCMP573, ADCMP580, ADCMP581, and ADCMP580.

## EVALUATION BOARD DESCRIPTION

Figure 1 is a photograph of the top of the evaluation board. It is fabricated using a high quality dielectric material between the ground plane and signal layers in order to maintain high signal integrity. All input and output signals are brought on to the board with 2.9 mm RF connectors, and transmission line paths are kept as close to 50  $\Omega$  as possible.

## PACKAGE LIST

- Evaluation board with component installed
- Schematic

## EVALUATION BOARD

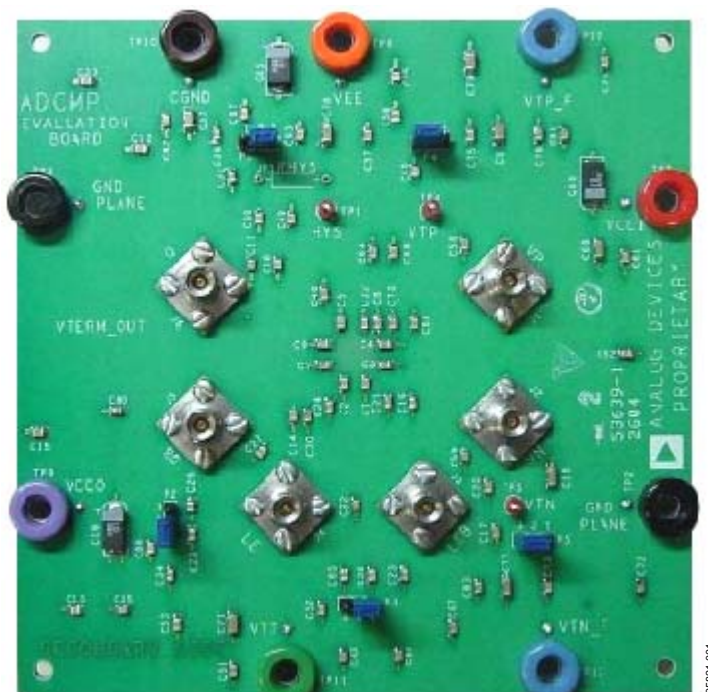


Figure 1. ADCMP572/ADCMP573/ADCMP580/ADCMP581/ADCMP582 Evaluation Board

### Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

## TABLE OF CONTENTS

General Description .....	1	Setup Input Signals.....	8
Evaluation Board Description.....	1	Connect Output Signals .....	8
Package List .....	1	Jumper Setup.....	9
Evaluation Board .....	1	Test Setup.....	10
Revision History .....	2	Additional Support.....	10
Using the Evaluation Board.....	3	Schematics .....	11
Measurements .....	3	Ordering Information.....	20
Setting Up the Evaluation Board .....	4	Ordering Guide .....	20
Connect Power.....	4	ESD Caution.....	20
Connect Inputs .....	8		

## REVISION HISTORY

2/06—Revision 0: Initial Version

## USING THE EVALUATION BOARD

### MEASUREMENTS

The same PCB is used to evaluate both ADCMP57x and ADCMP58x families. The Setting Up the Evaluation Board section describes the measurements that can be performed with this evaluation board.

**Table 1. Basic Equipment**

<b>Description</b>	<b>Example Equipment<sup>1</sup></b>	<b>Quantity</b>
Power Supply with Three Outputs	Agilent E3631A	2
Pulse Generator	HP8133A, Agilent 81134A	1
Signal Analyzer	CSA 8000 with 80E04 sampling head <sup>2</sup>	1
Source Meter	Keithley 2400 SourceMeter, Keithley 238 high current source-measure unit	1
Matched High Speed Cables with 2.9 mm Connectors	Insulated Wire Inc. kps-1501-180-kps Florida RF LABS LAB-FLEX 160 2Y194	4

<sup>1</sup> Equipment used to generate example measurements within this document.

<sup>2</sup> 20 GHz sampling head used for all time measurements.

# EVAL-ADCMP572/573/580/581/582

## SETTING UP THE EVALUATION BOARD

### CONNECT POWER

Several power supply levels must be provided to the board for  $V_{CC1}$ ,  $V_{CC0}$ ,  $V_{EE}$ ,  $V_{TT}$ , CGND (the comparator's GND pin), and GND via the banana jacks. Make a direct connection from the DUT output pins to the oscilloscope because any transmission line discontinuity degrades performance.

Because of this,  $V_{TT}$  is always at GND and therefore,  $V_{CC0} = V_{TT}$  (GND) + 2.0 V for the ECL/PECL ADCMP573/ADCMP581/ADCMP582, and  $V_{CC0} = V_{TT} = \text{GND}$  for the CML type ADCMP572 and  $\text{GND} = \text{CGND} = V_{TT}$  only for the CML ADCMP580, as detailed in **Table 2** through Table 4.

**Table 2. ADCMP580/ADCMP581 Power Supply Connections**

Pin No.	Mnemonic	ADCMP580 (CML) <sup>1</sup>	ADCMP581(NECL) <sup>2</sup>
5, 16	$V_{CC1}$ (Red)	5.0 V	7.0 V
9, 12	GND (Purple) (also CGND for these devices)	0.0 V	2.0 V
13	$V_{EE}$ (Orange)	-5.0 V	-3.0 V
14	HYS (Orange)	-5.0 V	-3.0 V
8	$V_{TT}$ (Green)	0 V	0 V
15	CGND (Brown) <sup>3</sup>	0.0 V	2.0 V
	GND Plane (Black) <sup>4</sup>	0 V	0 V

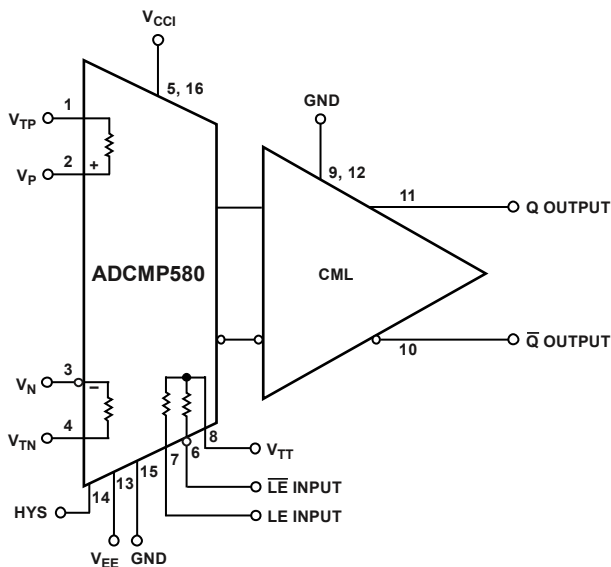
<sup>1</sup>  $V_{CC1} = 5.0 \text{ V}$ ,  $V_{CC0} = 0 \text{ V}$ ,  $V_{EE} = -5.0 \text{ V}$ .

<sup>2</sup>  $V_{CC1} = 5.0 \text{ V}$ ,  $V_{CC0} = 0 \text{ V}$ ,  $V_{EE} = -5.0 \text{ V}$ .

<sup>3</sup> CGND is the comparator ground (Pin 15) renamed.

<sup>4</sup> GND is always system ground.

The flexible power supply scheme of the ADCMP572/ADCMP573 comparators can be confusing with  $V_{TT}$  at system ground. The GND pin on the comparator is no longer at GND dc potential, except for the ADCMP580, and, therefore, is named CGND on the board.

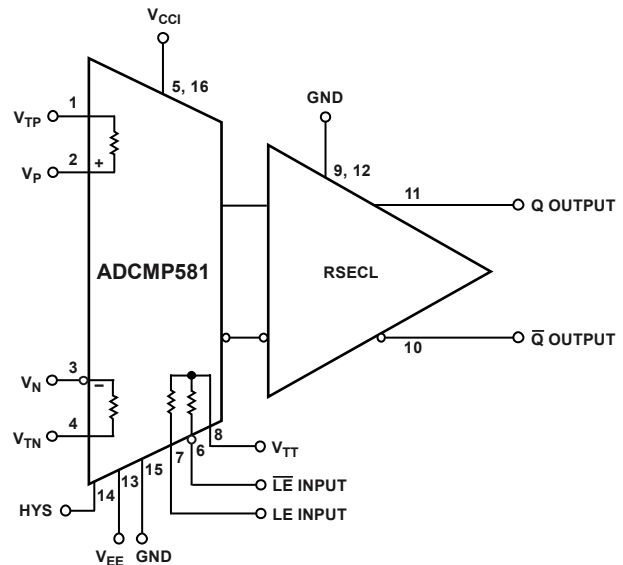


**NOTES**

1. FOR ADCMP580 CGND = GND.

Figure 2. ADCMP580 Power Supply Connections

05621-023



**NOTES**

1. GND HERE BECOMES BOARD CGND.

Figure 3. ADCMP581 Power Supply Connections

05621-024

**Table 3. ADCMP582 Power Supply Connections**

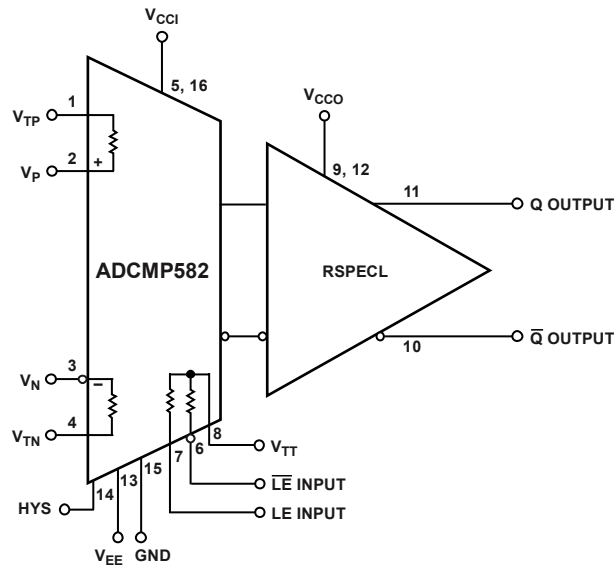
Pin No.	Mnemonic	ADCMP582(PECL) <sup>1</sup>	ADCMP582(PECL) <sup>2</sup>	ADCMP582(PECL)
5, 16	V <sub>CCI</sub> (Red)	2.0 V	3.7 V	4.5 V
9, 12	V <sub>CCO</sub> (Purple)	2.0 V	2.0 V	2.0 V
13	V <sub>EE</sub> (Orange)	-8.0 V	-6.3 V	-5.5 V
14	HYS	-8.0 V	-6.3 V	-5.5 V
8	V <sub>TT</sub> (Green)	0 V	0 V	0 V
15	CGND (Brown) <sup>3</sup>	-3.0 V	-1.3 V	-0.5 V
	GND Plane (Black) <sup>4</sup>	0 V	0 V	0 V

<sup>1</sup> V<sub>CCI</sub> = 5.0 V, V<sub>CCO</sub> = 5.0 V, V<sub>EE</sub> = -5.0 V.

<sup>2</sup> V<sub>CCI</sub> = 5.0 V, V<sub>CCO</sub> = 3.3 V, V<sub>EE</sub> = -5.0 V.

<sup>3</sup> CGND is the comparator ground (Pin 15) renamed.

<sup>4</sup> GND is always system ground.



**NOTES**

1. GND HERE BECOMES BOARD CGND.

Figure 4. ADCMP582 Power Supply Connections

05821-025

# EVAL-ADCMP572/573/580/581/582

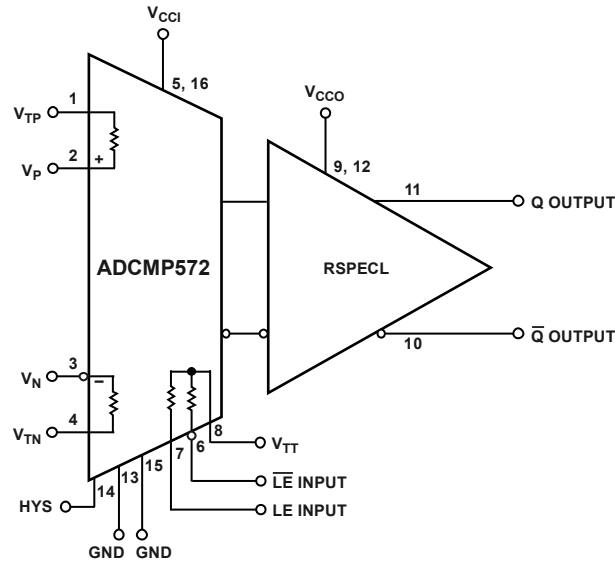
**Table 4. ADCMP572 Power Supply and Input Translation**

Pin	Case 1 <sup>1</sup>	Case 2 <sup>2</sup>	Case 3 <sup>3</sup>
V <sub>CCI</sub>	0.0 V	1.9 V	0.0 V
V <sub>CCO</sub>	0.0 V	0.0 V	0.0 V
CGND	-3.3 V	-3.3 V	-5.2 V
V <sub>TP_F</sub> /V <sub>TN_F</sub>	0 V	0 V	0 V
V <sub>TT</sub>	0.0 V	0.0 V	0.0 V
V <sub>P</sub> /V <sub>N</sub>	-3.5 V < V <sub>N</sub> /V <sub>P</sub> < -2.1 V	-3.5 V < V <sub>P</sub> /V <sub>N</sub> < -0.1 V	-5.4 V < V <sub>P</sub> /V <sub>N</sub> < -2.0 V
LE/ $\overline{\text{LE}}$	0.0 V/-0.4 V	0.0 V/-0.4 V	0.0 V/-0.4 V
AGND (This is not a pin in the part.)	0.0 V	0.0 V	0.0 V

<sup>1</sup> V<sub>CCI</sub> = V<sub>CCO</sub> = 3.3 V.

<sup>2</sup> V<sub>CCI</sub> = 5.2 V, V<sub>CCO</sub> = 3.3 V.

<sup>3</sup> V<sub>CCI</sub> = V<sub>CCO</sub> = 5.2 V.



**NOTES**

1. GND HERE BECOMES BOARD CGND.

Figure 5. ADCMP572 Power Supply Connections

06821-021

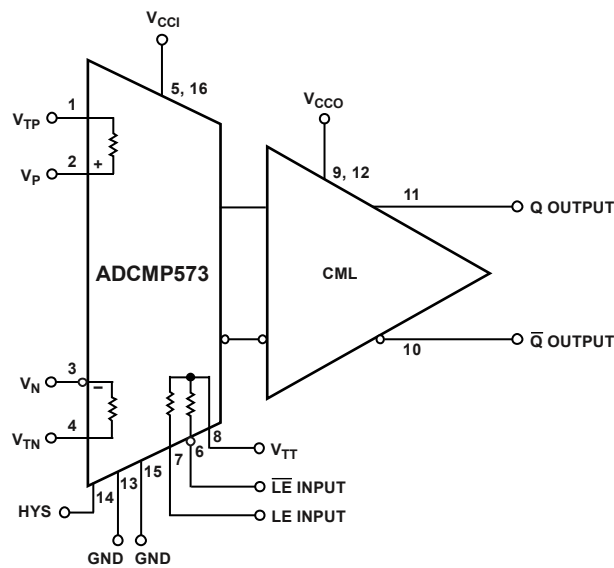
**Table 5. ADCMP573 Power Supply and Input Translation**

Pin	Case 1 <sup>1</sup>	Case 2 <sup>2</sup>	Case 3 <sup>3</sup>
V <sub>CCI</sub>	2.0 V	3.9 V	2.0 V
V <sub>CCO</sub>	2.0 V	2.0 V	2.0 V
CGND	-1.3 V	-1.3 V	-3.2 V
V <sub>TP_F</sub> /V <sub>TN_F</sub>	0 V	0 V	0 V
V <sub>TT</sub>	0.0 V	0.0 V	0.0 V
V <sub>P</sub> /V <sub>N</sub>	-1.5 V < V <sub>N</sub> /V <sub>P</sub> < -0.1 V	-1.5 V < V <sub>P</sub> /V <sub>N</sub> < +1.9 V	-3.4 V < V <sub>P</sub> /V <sub>N</sub> < 0.0 V
LE/ $\overline{\text{LE}}$	1.2 V/0.8 V	1.2 V/0.8 V	1.2 V/0.8 V
AGND	0.0 V	0.0 V	0.0 V
This is not a pin in the part.			

<sup>1</sup> V<sub>CCI</sub> = V<sub>CCO</sub> = 3.3 V.

<sup>2</sup> V<sub>CCI</sub> = 5.2 V, V<sub>CCO</sub> = 3.3 V.

<sup>3</sup> V<sub>CCI</sub> = V<sub>CCO</sub> = 5.2 V.



**NOTES**

1. GND HERE BECOMES BOARD CGND.

Figure 6. ADCMP573 Power Supply Connections

05821-02Z

# EVAL-ADCMP572/573/580/581/582

## CONNECT INPUTS

Connect the differential output of the generator to the differential comparator input pins of the device,  $V_P$  and  $V_N$ .

Connect the differential data output of the generator to the differential latch input of the device,  $\overline{LE}$  and  $\overline{LE}$ .

## SETUP INPUT SIGNALS

Input and latch levels must be shifted consistently with the power supplies (see Table 4 through Table 7).

Set voltage termination  $V_{TP\_F}$  and  $V_{TN\_F}$  to GND to terminate the on-chip, 50  $\Omega$  input resistors.

Leave the hysteresis control pin, HYS, open for zero hysteresis or connect the HYS pin to  $V_{EE}$  with a suitably sized resistor to add the desired amount of hysteresis.

## CONNECT OUTPUT SIGNALS

Connect the output of the comparator, Q and QB, to the signal analyzer. The sampling head must have an internal 50  $\Omega$  termination to ground.

**Table 6. ADCMP580/ADCMP581 Input Signal and Latch Setup**

Pin	Mnemonic	ADCMP580 (CML) <sup>1</sup>	ADCMP581 (NECL) <sup>2</sup>
2, 3	$V_P/V_N$	$-2.0\text{ V} < V_P/V_N < +3.0\text{ V}$	$0.0\text{ V} < V_P/V_N < +5.0\text{ V}$
1, 4	$V_{TP\_F}/V_{TN\_F}$ (Blue)	0V	0V
6, 7	$\overline{LE}/\overline{LE}$	0.0V/0.4V	0.8V/0.4V

<sup>1</sup>  $V_{CCI} = 5.0\text{ V}$ ,  $V_{CCO} = 0\text{ V}$ ,  $V_{EE} = -5.0\text{ V}$ .

<sup>2</sup>  $V_{CCI} = 5.0\text{ V}$ ,  $V_{CCO} = 0\text{ V}$ ,  $V_{EE} = -5.0\text{ V}$ .

**Table 7. ADCMP582 Input Signal and Latch Setup**

Pin	Mnemonic	ADCMP582(PECL) <sup>1</sup>	ADCMP582(PECL) <sup>2</sup>	ADCMP582(PECL) <sup>3</sup>
2, 3	$V_P/V_N$	$-5.0\text{ V} < V_P/V_N < 0.0\text{ V}$	$-3.3\text{ V} < V_P/V_N < 1.7\text{ V}$	$-2.5\text{ V} < V_P/V_N < 2.5\text{ V}$
1, 4	$V_{TP\_F}/V_{TN\_F}$ (Blue)	0V	0V	0V
6, 7	$\overline{LE}/\overline{LE}$	0.8V/0.4V	0.8V/0.4V	0.8V/0.4V

<sup>1</sup>  $V_{CCI} = 5.0\text{ V}$ ,  $V_{CCO} = 5.0\text{ V}$ ,  $V_{EE} = -5.0\text{ V}$

<sup>2</sup>  $V_{CCI} = 5.0\text{ V}$ ,  $V_{CCO} = 3.3\text{ V}$ ,  $V_{EE} = -5.0\text{ V}$

<sup>3</sup>  $V_{CCI} = 5.0\text{ V}$ ,  $V_{CCO} = 2.5\text{ V}$ ,  $V_{EE} = -5.0\text{ V}$



## JUMPER SETUP

This evaluation board works with five different comparators, the ADCMP572/ADCMP573 and the ADCMP580/ADCMP581/ADCMP582. To reduce the number of wires to the power supply, jumpers are provided wherever comparator supplies might be rerouted. When a comparator is mounted onto the board, the jumpers should be set properly for that product. The user does not have to adjust Jumper 1, Jumper 2, and Jumper 3 unless a new device type is soldered onto the board.

If the evaluation board is to be used for a different comparator type than was mounted on the board originally, pull all the jumpers to prevent errors. Once the new part type is installed, the jumpers can be reinstalled. Table 8 gives the correct jumper settings and resulting banana jack connections for each of the comparator products. Set conservative current limits on all power supplies.

**Table 8. Jumper Connections**

Jumper	ADCMP572/ADCMP573	ADCMP580/ADCMP581	ADCMP582	Conditions
P1	Short 1, 2 (TP10)	Short 2, 3 (TP6)	Short 2, 3 (TP6)	Device $V_{EE}/GND$
P2	Short 2, 3 (TP9)	Short 1, 2 (TP10)	Short 2, 3 (TP9)	Device $V_{CCO}$
P3	Short 1, 2 (TP2/GND)	Short 1, 2 (TP2/GND)	Short 1, 2 (TP2/GND)	Device $V_{TT}$
P4/P5	Short 2, 3	Short 2, 3	Short 2, 3	$V_P/V_N$ as a differential input
P4	Short 2, 3	Short 2, 3	Short 2, 3	Drive $V_P$
	Short 1, 2	Short 1, 2	Short 1, 2	Drive $V_N$
P5	Short 1, 2	Short 1, 2	Short 1, 2	DC Bias $V_N$
	Short 2, 3	Short 2, 3	Short 2, 3	DC Bias $V_P$

# EVAL-ADCMP572/573/580/581/582

## TEST SETUP

Figure 2 shows Analog Devices' test configuration setup that was used for much of the initial engineering evaluation. It is provided here as a guideline and to assist in replicating our setup.

## ADDITIONAL SUPPORT

For further support regarding the ADCMP572/ADCMP573 and ADCMP580/ADCMP581/ADCMP582 comparators and/or evaluation boards, refer to [www.analog.com](http://www.analog.com).

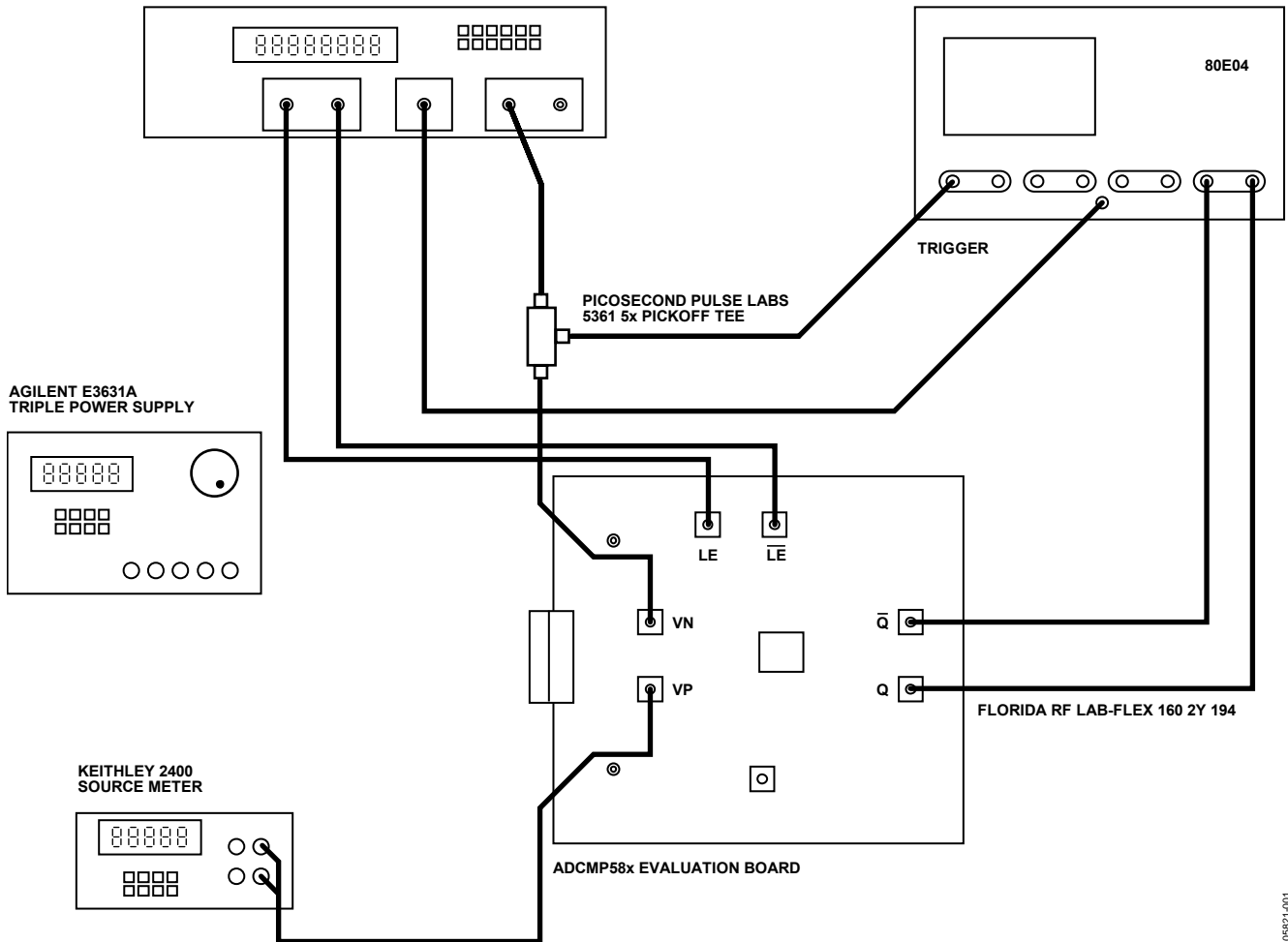


Figure 7. Typical Test Setup for Measuring Performance

05821-001

SCHEMATICS

- NOTES
1. OUTPUT SWING WILL BE APPROXIMATELY 400 mV<sub>p-p</sub> AS SEEN AT THE CONNECTOR INTO A 50 Ω LOAD.
  2. 2.9mm CONNECTOR MOUNTING SCREWS WILL NEED ADHESIVE.
  3. A SELECTION OF RESISTORS TO BE PROVIDED FOR POSSIBLE INSERTION INTO JP1.
  4. MAKE JP1'S MOUNTING HOLES LARGE ENOUGH FOR COTD CUPS.
  5. 0µA-500µA FLOATING/OPEN IS NORMAL OPERATING MODE.

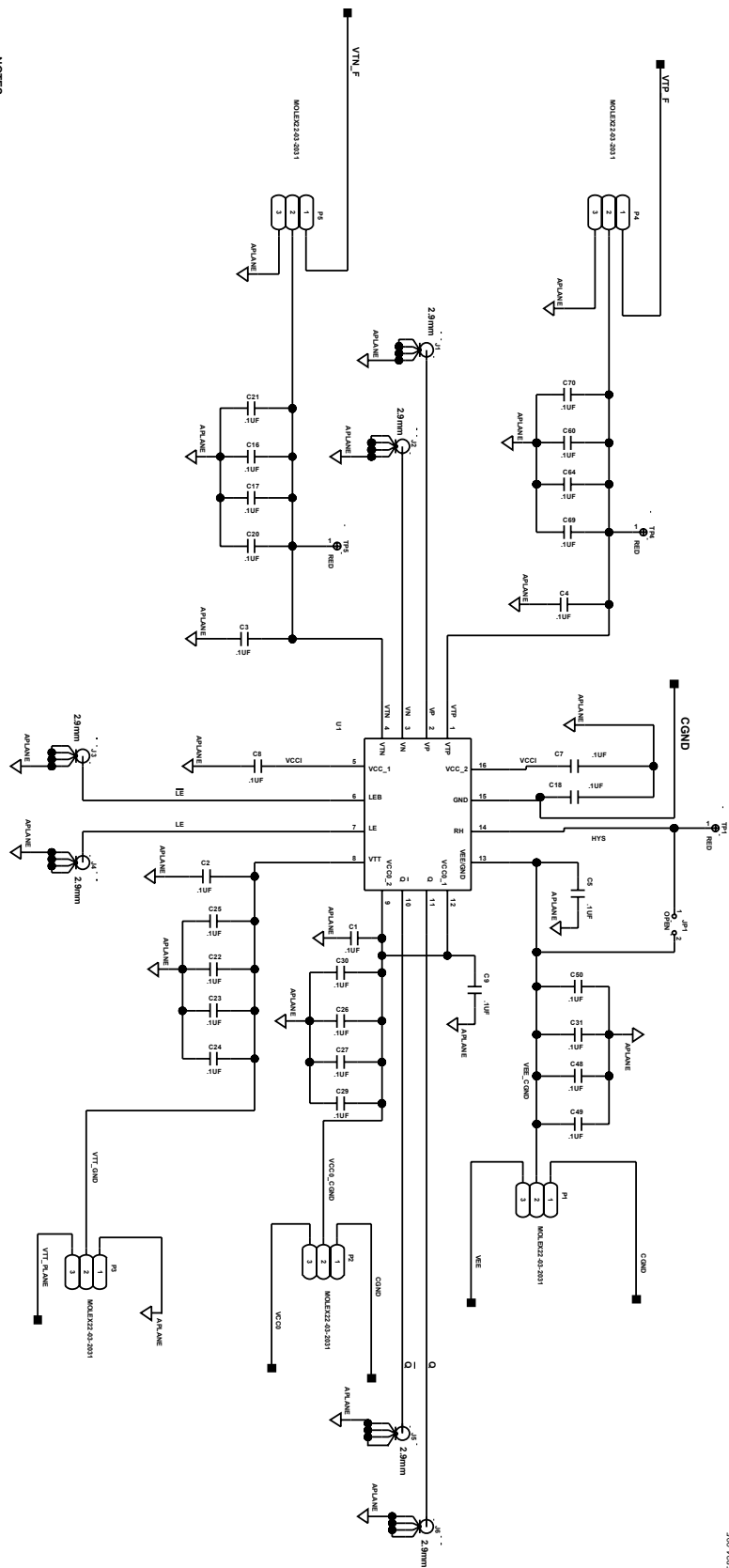


Figure 8. Schematic, Main

500-15950

# EVAL-ADCMP572/573/580/581/582

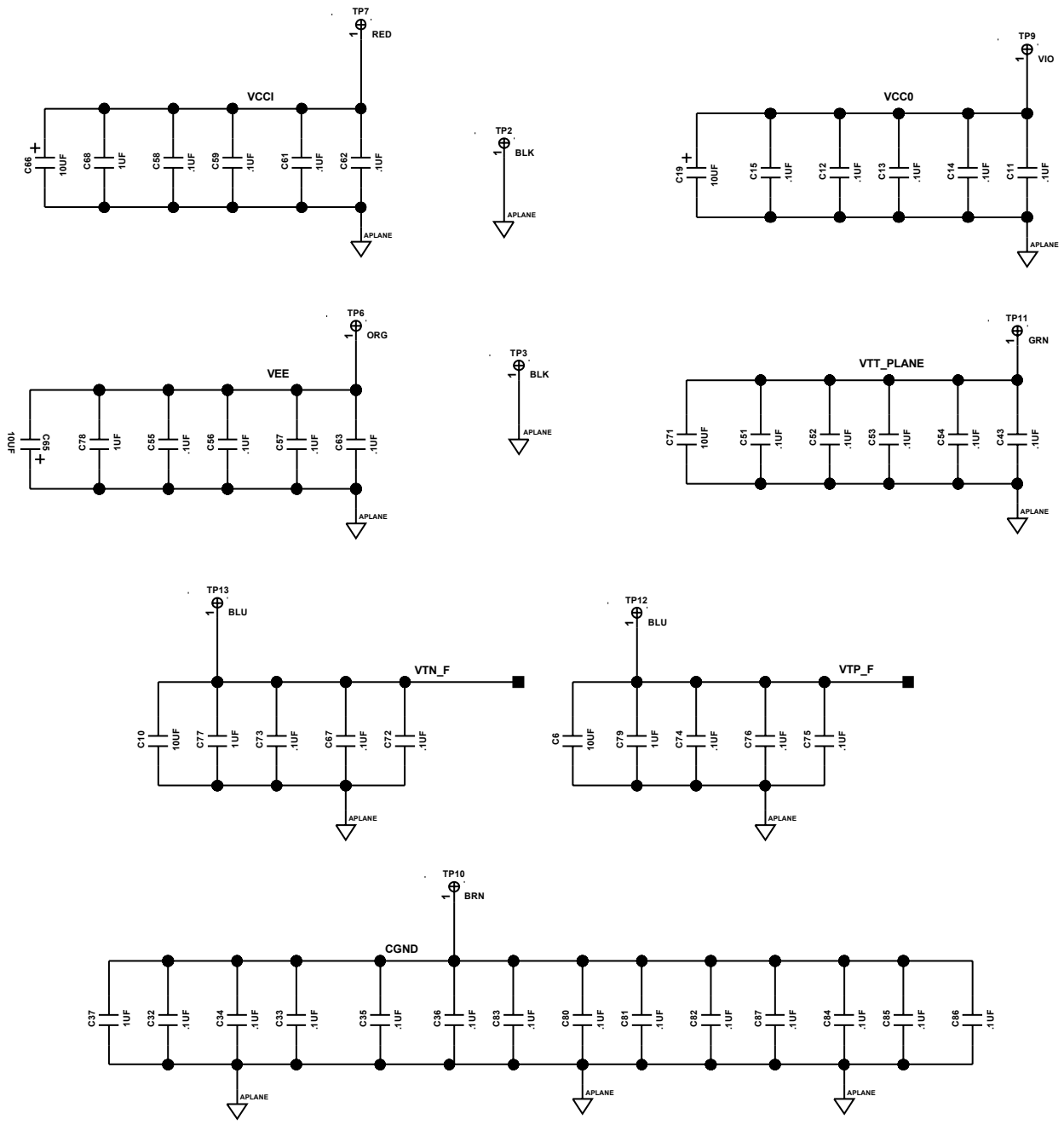


Figure 9. Schematic, Bypass Capacitors

06921-006

PC BOARD

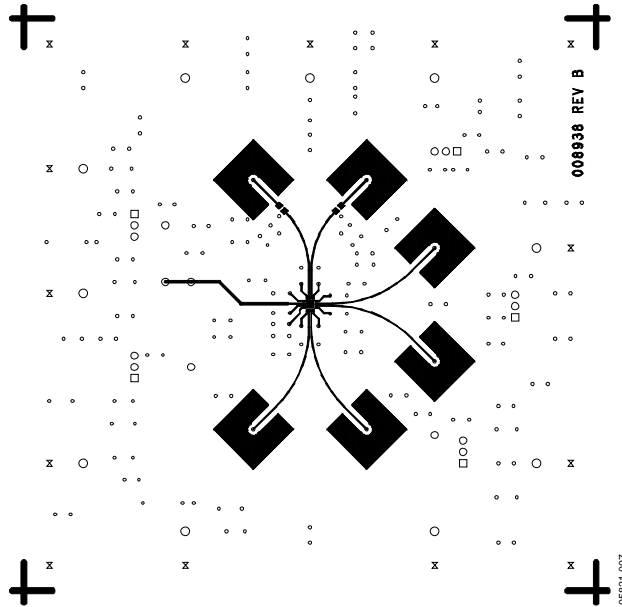


Figure 10. Bottom Signal Layer

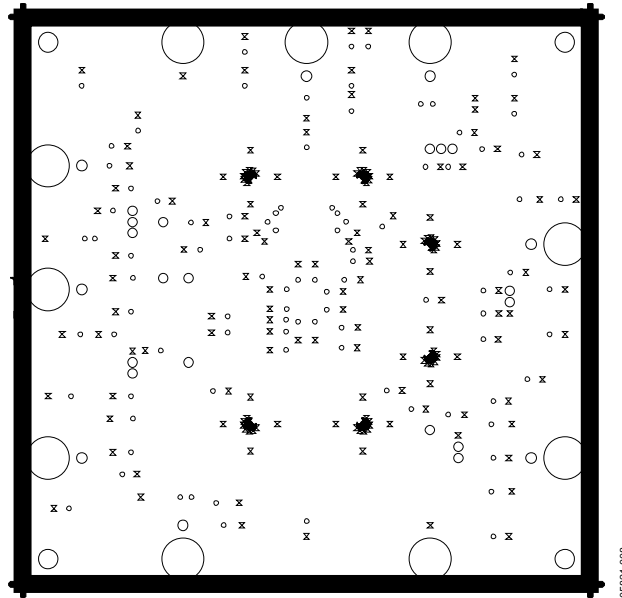


Figure 11. GND Plane

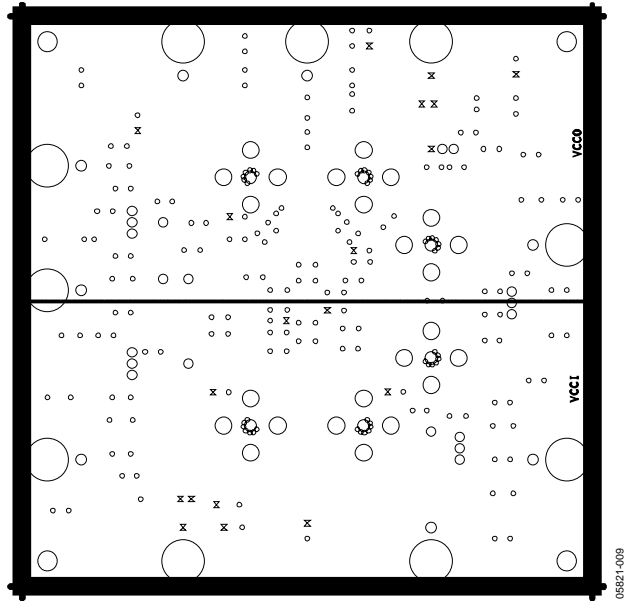


Figure 12. V<sub>CC</sub> Plane

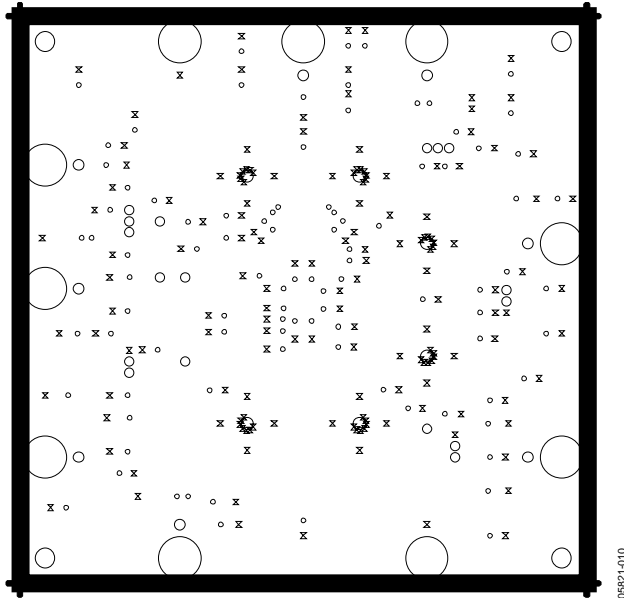


Figure 13. GND Plane

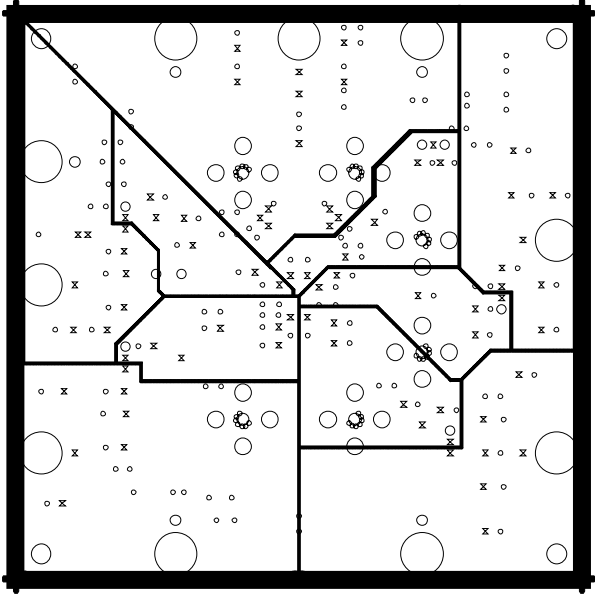


Figure 14. Miscellaneous DC Plane

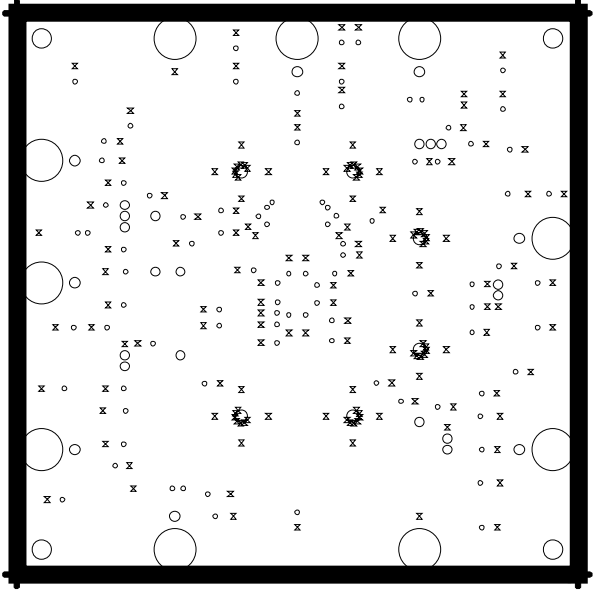
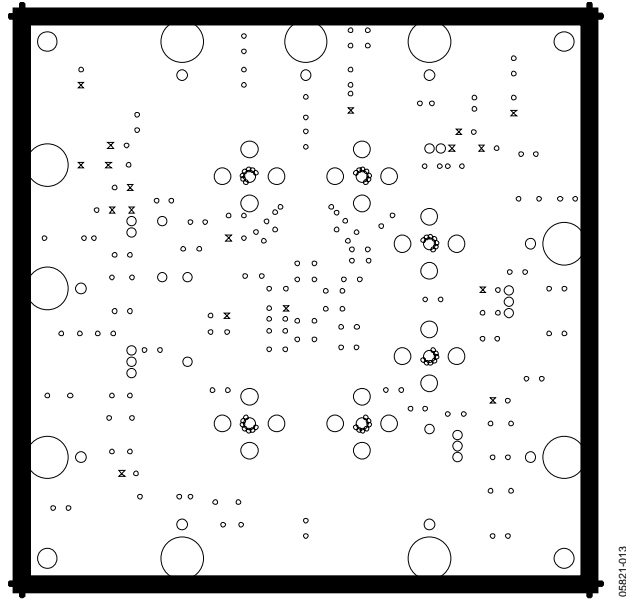
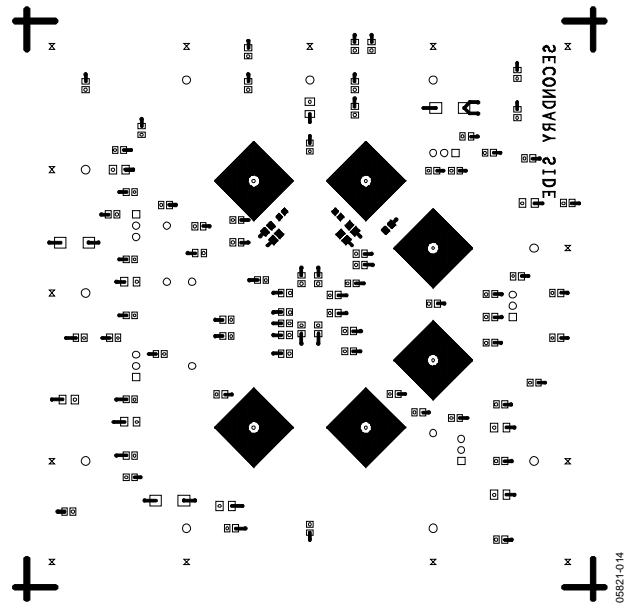


Figure 15. GND Plane



06821-013

Figure 16. Upper Plane



06821-014

Figure 17. Top



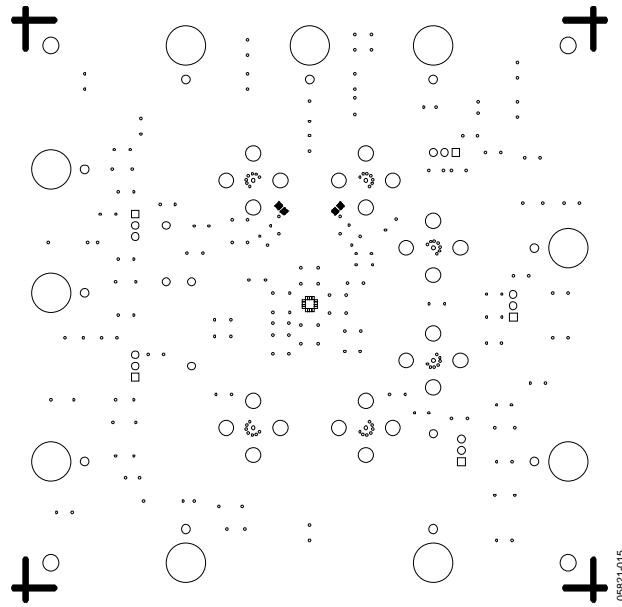


Figure 18. Solder Mask

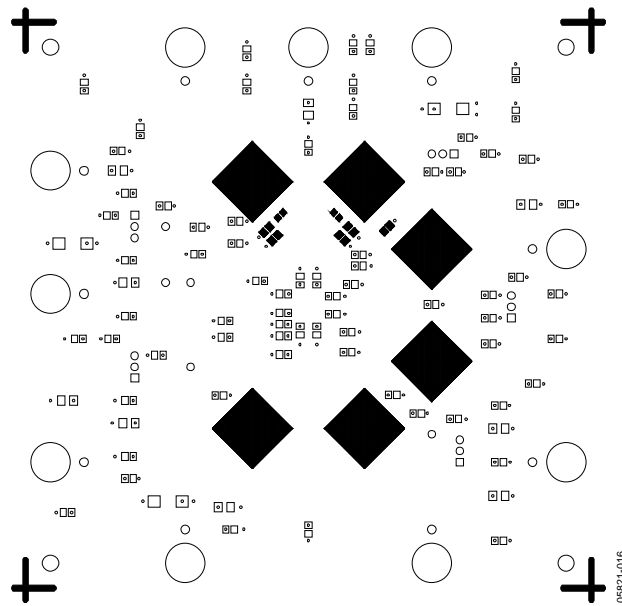


Figure 19. Solder Mask

# EVAL-ADCMP572/573/580/581/582

## SILKSCREENS

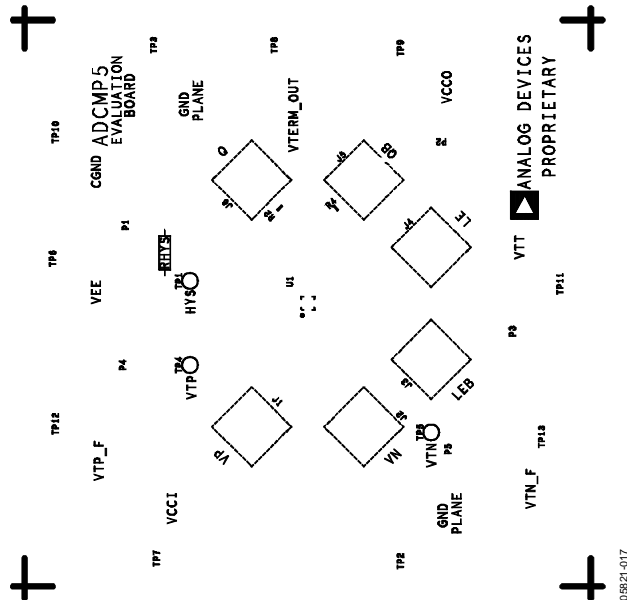


Figure 20. Silkscreen Bottom

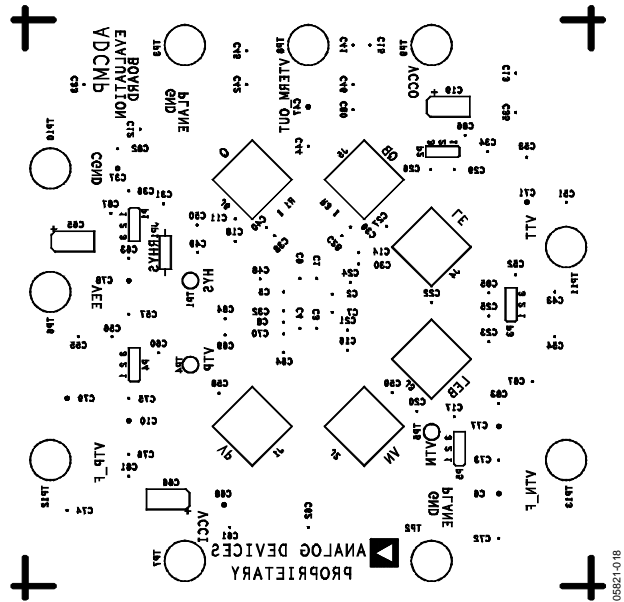


Figure 21. Silkscreen Top

# COMPONENTS

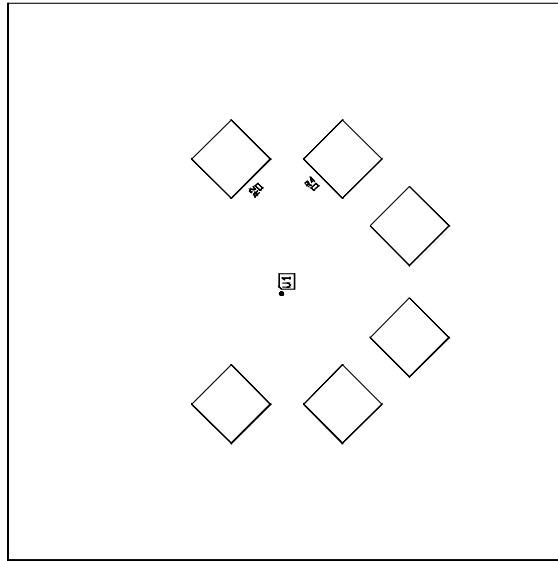


Figure 22 Bottom Components

05821-019

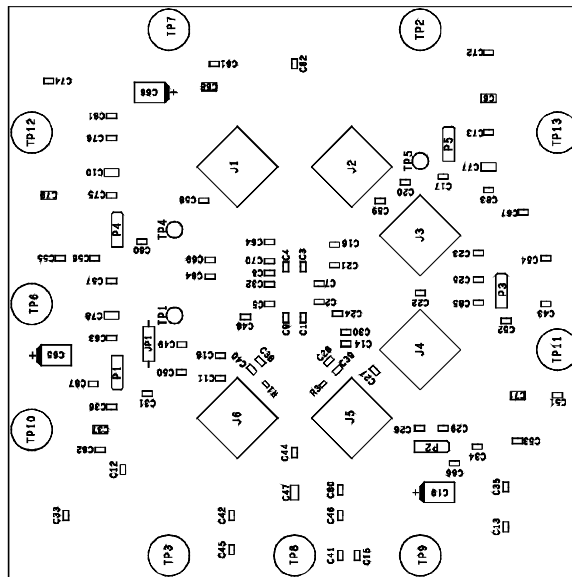


Figure 23. Top Components

05821-020

# EVAL-ADCMP572/573/580/581/582

## ORDERING INFORMATION

### ORDERING GUIDE

Model	Package Description
EVAL-ADCMP572BCP	Evaluation Board
EVAL-ADCMP573BCP	Evaluation Board
EVAL-ADCMP580BCP	Evaluation Board
EVAL-ADCMP581BCP	Evaluation Board
EVAL-ADCMP582BCP	Evaluation Board

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

