ISL78420EVAL1Z Evaluation Board User Guide

Description

The ISL78420EVAL1Z evaluation board is designed for a user to evaluate the ISL78420 100V 2A half-bridge driver with tri-level PWM input for driving the gates of two NMOS FETs in a half-bridge configuration. These NFET MOSFETs are included on the evaluation board to evaluate a half-bridge driven load such as a DC motor or a synchronous switching regulator.

The ISL78420 is offered in a 14 Ld HTSSOP package enhanced with a thermal EPAD. It operates from a supply voltage of 8V to 14V DC with the capability of driving a high-side NMOS FET in a 100V half-bridge configuration. A unique tri-level PWM input allows control of both the high and low-side gate driver with a single input. When the PWM pin is left in a floating high impedance state both gate drivers are turned off, which is beneficial for multiphase DC/DC switching that requires phase shedding.

Specifications

This board is optimized for the following operating conditions:

- VDD supply: 8V to 14V
- PWM switching frequency: 10kHz to 1MHz
- Preset half-bridge dead time: 35ns
- Peak gate drive current: 2A source and sink
- Half-bridge voltage: Up to 100V

Key Features

- 2A source and sink NMOS gate drivers
- Internal level shifter and bootstrap diode for gate driver on high-side FET
- Up to 100V high-side gate drive reference
- 8V to 14V bias supply operation
- Single PWM input for high-side and low-side gate driver with tri-level for turning off both drivers
- Single resistor adjustable dead time from 35ns to 220ns

Reference Documents

- ISL78420 datasheet
- ISL78225 datasheet
- AN1727, “ISL78225EVAL1Z: 4-Phase Interleaved Synchronous Boost Converter”

Ordering Information

PART NUMBER	DESCRIPTION
ISL78420EVAL1Z	Evaluation Board, 100V 2A Half-Bridge Driver with Tri-Level Input

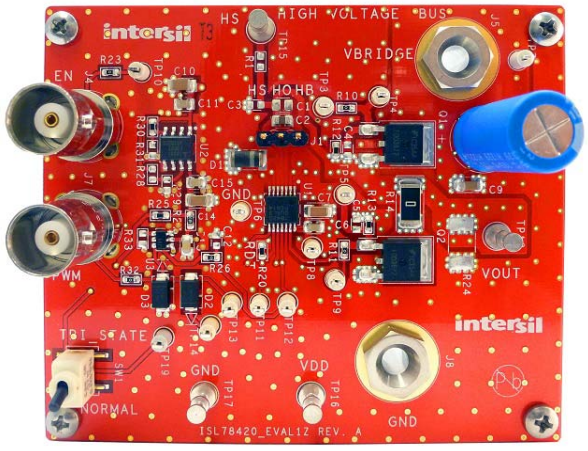

FIGURE 1. ISL78420EVAL1Z EVALUATION BOARD

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Recommended Equipment

The following equipment is recommended to operate this board:

- 8V to 14V power supply with at least 2A source current capability
- 0V to 100V power supply for biasing the half bridge
- Digital multimeters (DMMs)
- Up to 1MHz square wave generator
- Load such as a DC motor or buck regulator output stage (optional)

Quick Setup Guide

1. The dead time of the HO and LO signal is set to 35ns with an 80kΩ resistor from the RDT pin to GND. To change the dead time, replace the resistor at R20 with the value corresponding to the desired dead time. See Figure 9.
2. Apply 10V to 14V to VDD and GND.
3. Connect EN BNC to a function generator to control the enable of the ISL78420 or connect to VDD to always enable.
4. If evaluating the bridge circuit, connect a bridge supply <100V to the banana jack connectors J5 and J8. Connect load at R24.
5. Connect a 0V to 5V <1MHz PWM signal to J7.
6. Verify HO and LO outputs are switching. LO switches between GND and VDD phase inverted from PWM. HO switches between GND and V_{HB} + V_{BRIDGE} in phase with PWM.

Bootstrap Capacitor

The ISL78420 requires an external bootstrap capacitor between the HB and HS pins to provide the high-side supply biasing to generate the level shifted gate voltage on the HO pin and more importantly, deliver the gate drive current to switch the high-side NMOS FET.

The ISL78420EVAL1Z is populated with a 0.47µF capacitor at C2 for the bootstrap function. This value will provide optimal bias for switching frequencies ≥10kHz and is capable of delivering the dynamic current for 100nC total gate charge while maintaining <5% ripple voltage. See page 10 of the ISL78420 datasheet for optimizing the bootstrap capacitance at different operating conditions.

Dead Time Control

The ISL78420 features a dead time control circuit for programming the delay between the falling edge of HO to rising edge of LO and between the falling edge of LO to rising edge of HO. A single resistor from the RDT pin to GND adjusts the dead time from 35ns (80kΩ) to 220ns (8kΩ). The ISL78420EVAL1Z contains a 80kΩ resistor at R20 which sets the dead time to 35ns. Refer to Figure 9 for selecting a resistor value for the desired dead time.

Tri-Level Input

The ISL78420 has a single input pin (PWM) for controlling the HO/LO high-side and low-side gate drivers. See Table 1 below for logic table of PWM to HO and LO. When the PWM pin is left floating or driven to a valid tri-level voltage, both HO and LO outputs are driven low.

Because some function generators do not have a high impedance disable function (when disabled, the generator output pulls to GND), the ISL78420EVAL1Z has a switch SW1 on board to isolate the function generator signal to the PWM input. Otherwise, the PWM signal is taken to ground which keeps the LO output at VDD voltage and the HO ouput at HS voltage.

TABLE 1. TRI-LEVEL PWM LOGIC INPUT

PWM	GATE DRIVE	HO/LO OUTPUT VOLTAGE
HIGH	HO	Driven to HB+HS
	LO	Driven to VSS
MID	HO	Driven to HS
	LO	Driven to VSS
LOW	HO	Driven to HS
	LO	Driven to VDD

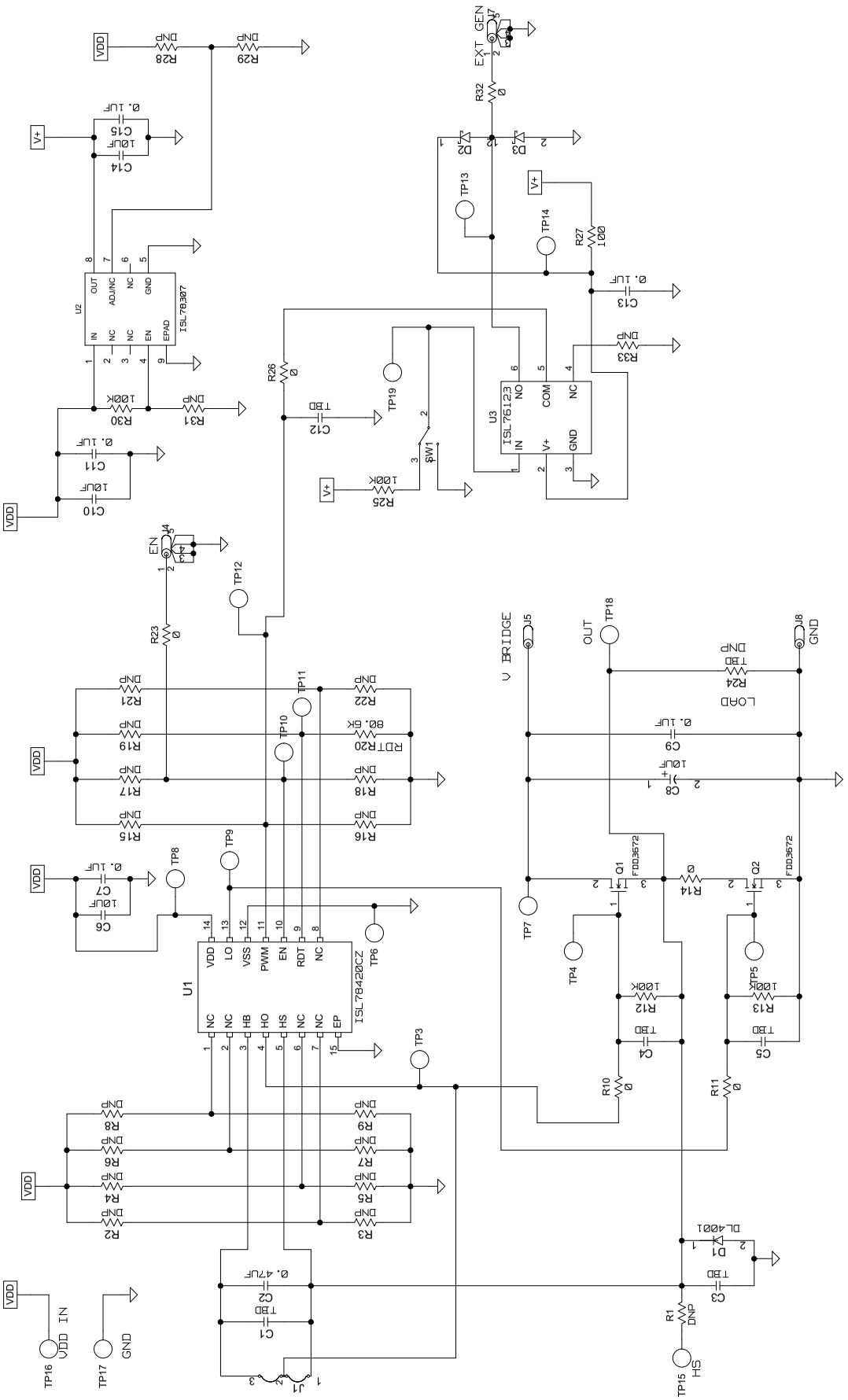
Half Bridge Configured MOSFETs

The ISL78420EVAL1Z includes a bridge configured high side (Q1) and low side (Q2) FET. These devices are automotive grade 100V NMOS FETs. The source of the high-side FET and drain of the low-side FET are connected together to the HS node of the ISL78420. The HO pin drives the gate of Q1 and the LO pin drives the gate of Q2. The 0.47µF boot capacitor is designed to provide the necessary gate drive to switch Q1 to frequencies down to 10kHz with minimal ripple on the bootstrap bias.

Other Circuits

The ISL78420EVAL1Z also contains an automotive grade LDO (ISL78307) and SPDT switch (ISL76123) which is used to switch between the PWM signal external to the ISL78420 or have the signal path open, allowing the ISL78420 PWM pin to float to a tri-level state. The ISL78307 LDO accepts the 10V to 14V VDD input voltage and outputs a constant 5V bias for the ISL76123 analog switch that connects or disconnects the signal at J7 BNC from the PWM pin of ISL78420. The switch SW1 toggles the logic state of the ISL76123.

ISL78420EVAL1Z Schematic



BILL OF MATERIALS

PART NUMBER	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER
ISL78420AVEZ	U1	100V; 2A BRIDGE DRIVER	INTERSIL
ISL76123AHZ	U3	300mA SPDT SWITCH; SOT26	INTERSIL
ISL78307FBEBZ	U2	40V; 50mA LDO; SOIC	INTERSIL
10MQ060N	D2, D3	2.1A 60V SCHOTTKY	IR
DL4001	D1	50V; 1A DIODE	MCC
FDD3672	Q1, Q2	NFET 100V, 44A,28mΩ, TO-252	FAIRCHILD
GT11MSCBETR	SW1	SPDT SWITCH	C&K
UBT2D100MPD1TD	C8	10µF CAP; 200V; 20%; RADIAL	NICHICON
	C6, C10, C14	10µF CAP; 50V; 10%; 1206	GENERIC
	C7, C11, C13, C15	0.1µF CAP; 50V; 5%; 0805	GENERIC
	C2	0.47µF CAP; 50V; 10%; 0805	GENERIC
	C9	0.1µF CAP; 200V; 10%; 1206	GENERIC
	R10, R11, R23, R26, R32	0Ω; 1/16W; 1%; 0603	GENERIC
	R27	100Ω; 1/16W; 1%; 0603	GENERIC
	R12, R13, R25, R30	100kΩ; 1/16W; 1%; 0603	GENERIC
	R20	80.6kΩ; 1/16W; 1%; 0603	GENERIC
	R14	0Ω; 1W; 1%; 2512	GENERIC
	TP3-TP19	TEST POINT	
	J5, J8	BANANA JACK	
	J4, J7	BNC CONNECTOR	
PCB SPECIFICATION		2oz Cu; 1.57mm Thickness FR-4	

ISL78420EVAL1Z Board Layout

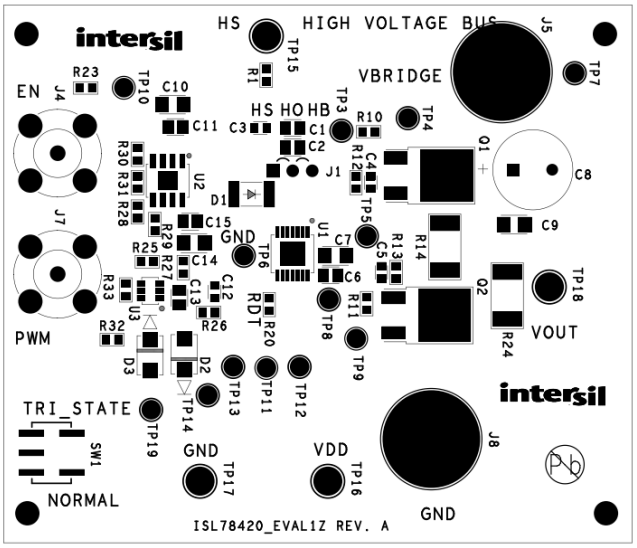


FIGURE 2. SILK SCREEN TOP

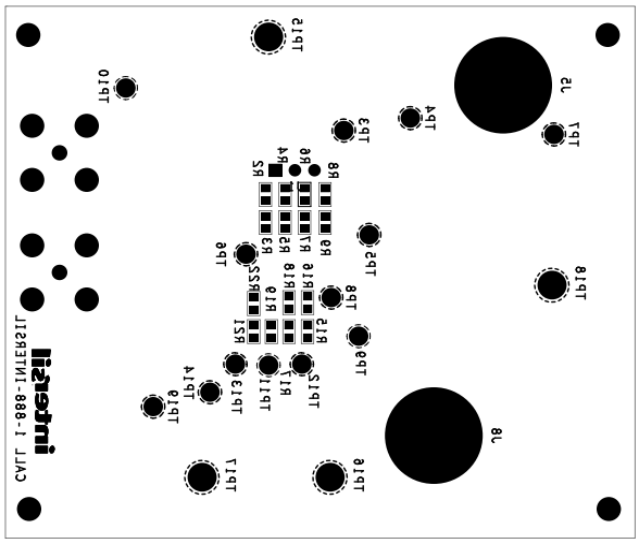


FIGURE 3. SILK SCREEN BOTTOM

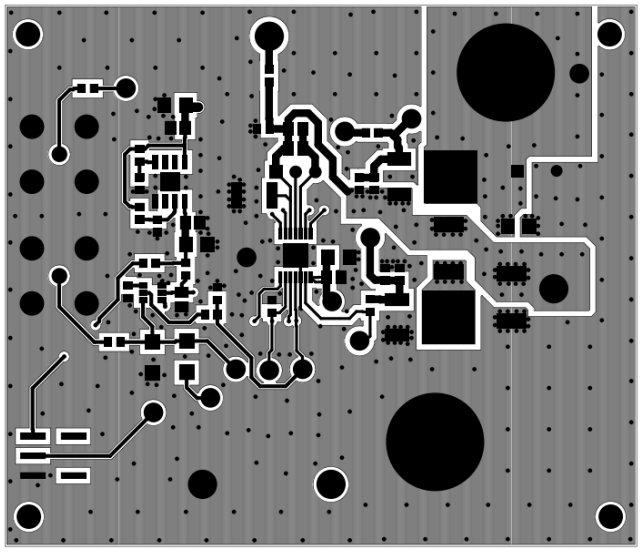


FIGURE 4. TOP LAYER PCB

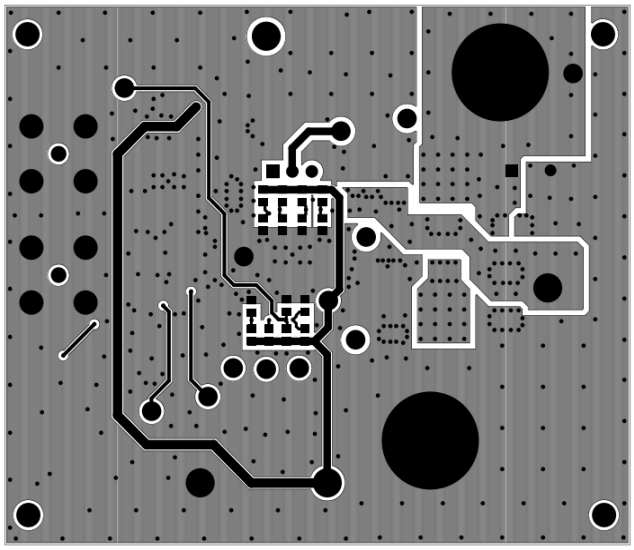


FIGURE 5. BOTTOM LAYER PCB

Typical Performance Curves

Unless otherwise specified, operating conditions at: T = 25°C; V_{DD} = EN = 12V; V_{SS} = HS = 0V; RDT = 10kΩ; C_{BOOT} = 0.47µF; 100kΩ load on LO to VSS and HO to HS.

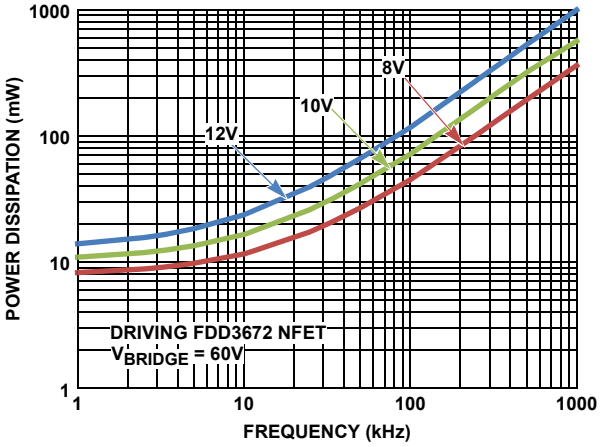


FIGURE 6. POWER DISSIPATION vs FREQUENCY vs VDD with NFET LOAD

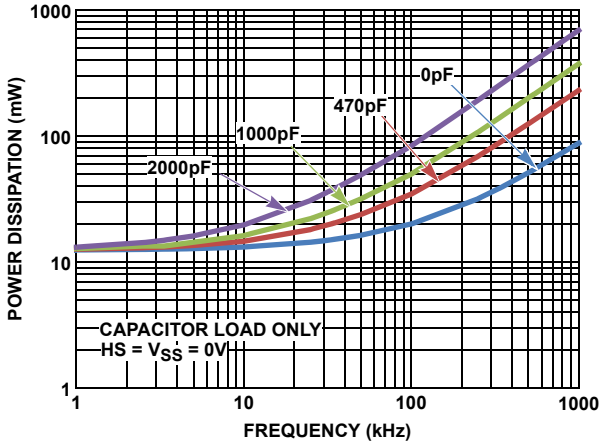


FIGURE 7. POWER DISSIPATION vs FREQUENCY vs CAPACITIVE LOAD

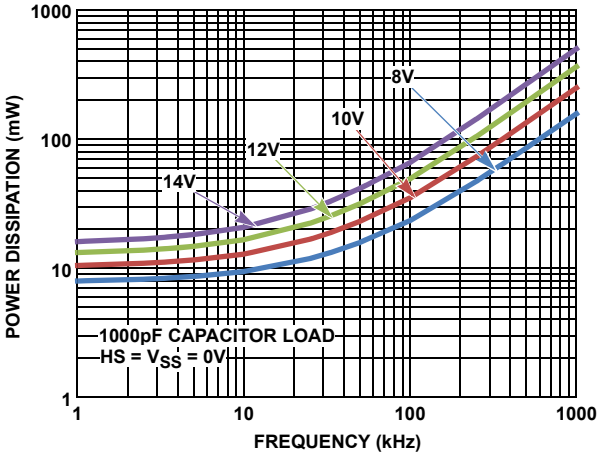


FIGURE 8. POWER DISSIPATION vs FREQUENCY vs VDD

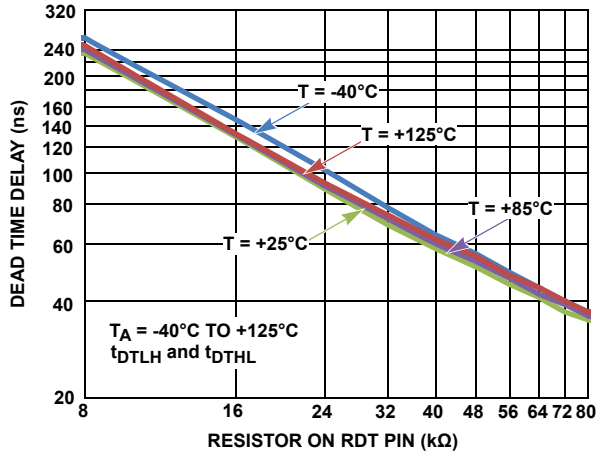


FIGURE 9. DEAD TIME DELAY vs RDT RESISTOR

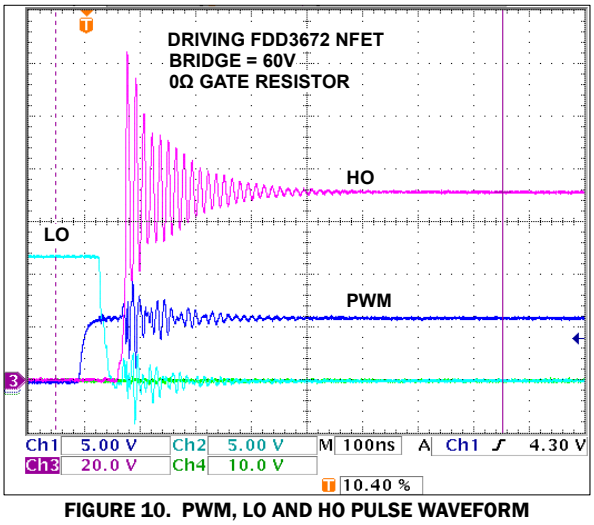


FIGURE 10. PWM, LO AND HO PULSE WAVEFORM

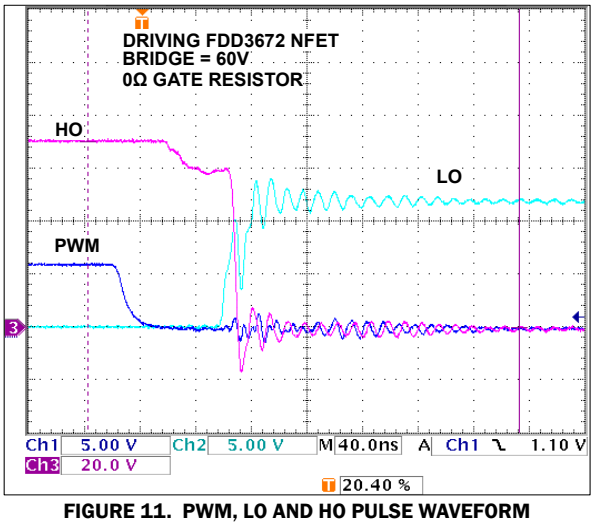


FIGURE 11. PWM, LO AND HO PULSE WAVEFORM

Typical Performance Curves

Unless otherwise specified, operating conditions at: T = 25°C; V_{DD} = EN = 12V; V_{SS} = HS = 0V; RDT = 10kΩ; C_{BOOT} = 0.47µF; 100kΩ load on LO to VSS and HO to HS. **(Continued)**

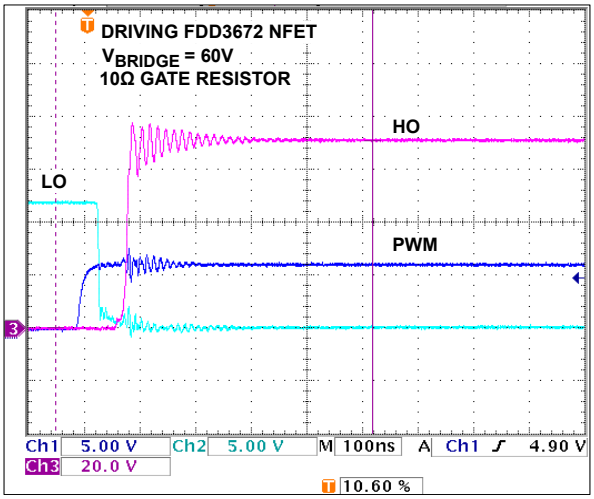


FIGURE 12. PWM, LO AND HO PULSE WAVEFORM

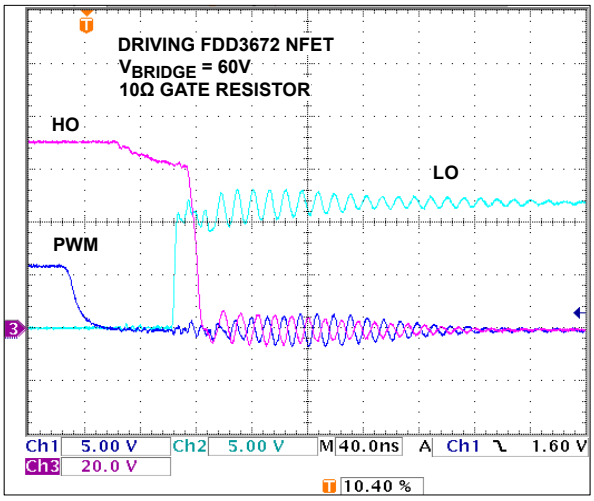


FIGURE 13. PWM, LO AND HO PULSE WAVEFORM

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