

SP5002 Series 6 Channel Common Mode Filter with ESD Protection    

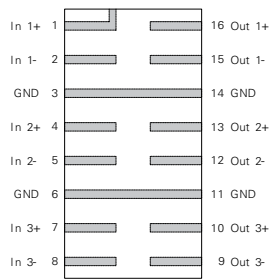


Description

The SP5002 Series is a highly integrated Common Mode Filter (CMF) providing both ESD protection and EMI common mode noise filtering for systems using high speed differential serial interfaces, such as MIPI D-PHY.

The SP5002 Series can protect and filter three differential line pairs in a small RoHS-compliant TDFN-16 package, with cost and space savings over discrete solutions.

Pinout

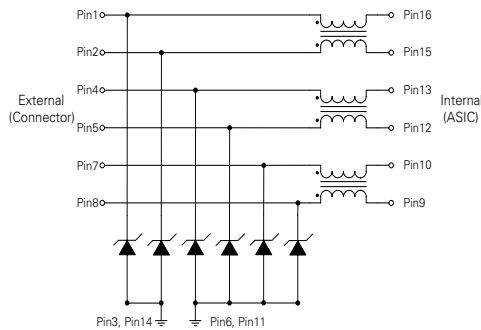


Note :This drawing is not to scale.

Features

- Large differential bandwidth > 2GHz
- High Common Mode Stop Band Attenuation:
 - > 25 dB at 700 MHz
 - > 30 dB at 800 MHz
- ±15kV ESD protection per channel (IEC 61000-4-2 Level 4, contact discharge)
- TDFN-16 4.00mm × 2.00mm × 0.75mm package with 0.50mm lead pitch
- RoHS-compliant, Lead-free packaging
- AEC-Q101 qualified
- Moisture Sensitivity Level (MSL) 1

Functional Block Diagram



Applications

- MIPI D-PHY (CSI-2, DSI, etc) in Mobile Phones and Digital Still Cameras

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{DC}	DC Current Per Line	100	mA
P_{DC}	DC Package Power Rating	0.5	W
T_{OP}	Operating Temperature	-40 to 125	°C
T_{STOR}	Storage Temperature	-55 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

Parameter	Rating	Units
Storage Temperature Range	-55 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

Electrical Characteristics ($T_{OP}=25^{\circ}C$)

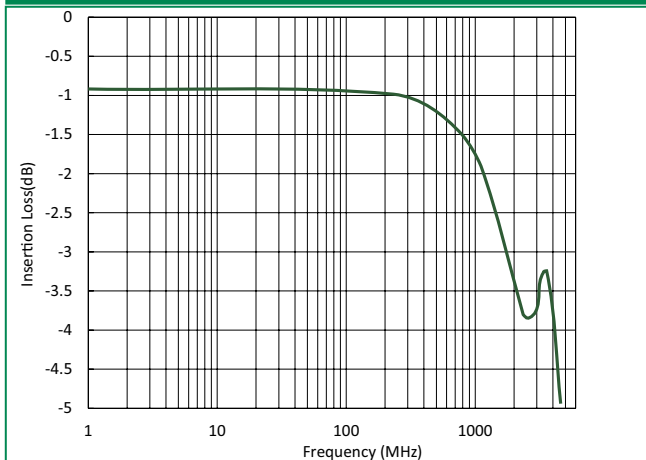
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Channel Resistance	R_{CH}	Pins 1-10, 2-9, 4-7 and 5-6		8.0		Ω
Total Channel Capacitance	C_{TOTAL}	$V_{IO} = 1.65V_{DC}$ Reverse Bias; $f=1MHz, 30mV_{AC}$		0.8	1.3	pF
Reverse Standoff Voltage	V_{RWM}				5.0	V
Breakdown Voltage	V_{BR}	$I_T=1mA$	6.0	8.0	10.0	V
Forward Voltage at I_F	V_F	$I_F=1mA$	0.4	0.7	1.5	V
Reverse Leakage Current	I_{LEAK}	$V_{IO}=3.3V$		0.01	0.10	μA
Dynamic Resistance ^{2,3}	R_{DYN}	Positive (tp=8/20 μs)		1.3		Ω
		Negative (tp=8/20 μs)		0.7		
		TLP, tp=100ns, I/O to GND		0.36		
ESD Withstand Voltage ^{1,2}	V_{ESD}	IEC61000-4-2 (Contact Discharge)	± 15			kV
		IEC61000-4-2 (Air Discharge)	± 30			kV
Differential Mode Cutoff Frequency ²	F_{3dB}	$Z_{SOURCE}=50\Omega, Z_{LOAD}=50\Omega$		2.0		GHz
Common Mode Stop Band Attenuation ²	F_{α}	$f=800MHz$		30		dB

Notes: ¹ ESD zapping at I/O pins (1,2,4,5,7,8) with respect to GND.

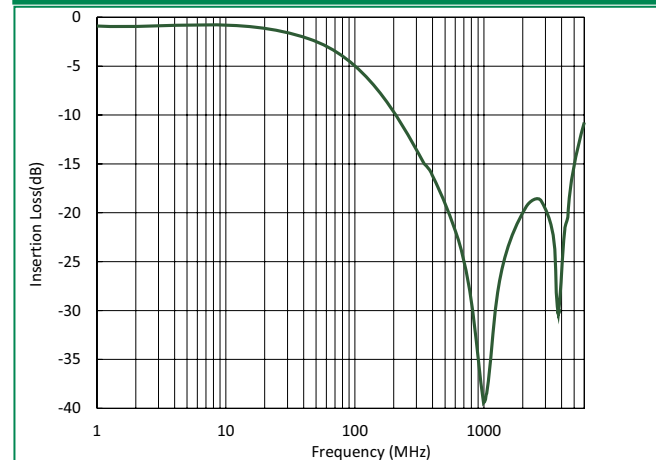
² Guaranteed by design.

³ Transmission Line Pulse (TLP) with 100ns width and 200ps rise time.

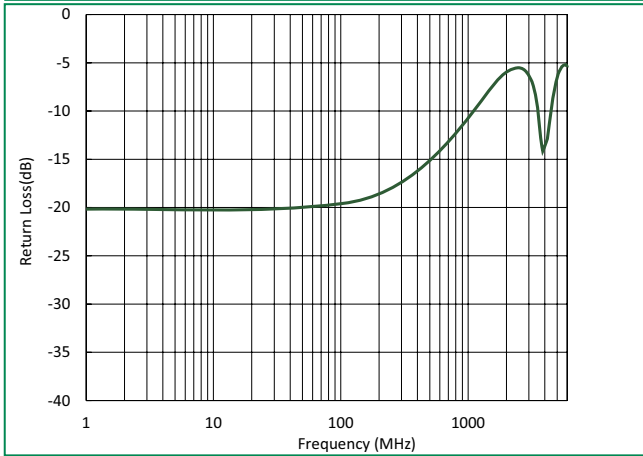
Differential Mode Attenuation SDD21 vs. Frequency (Zdiff = 100 Ω)



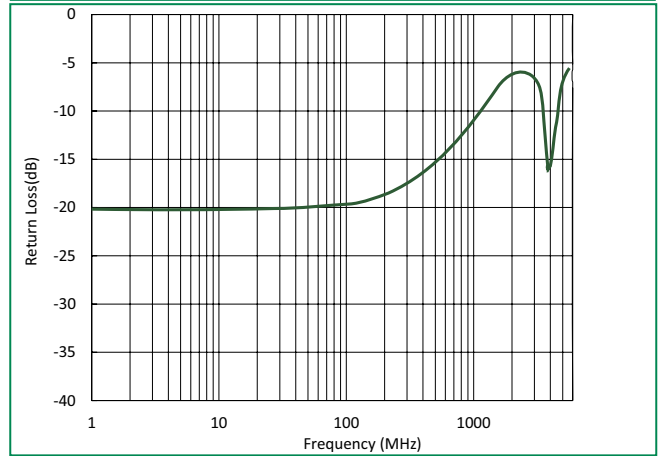
Common Mode Attenuation SCC21 vs. Frequency (Zcomm = 50 Ω)



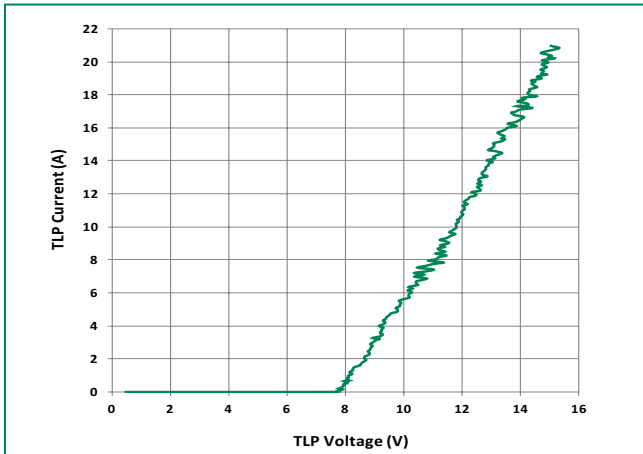
Differential Return Loss SDD11 vs. Frequency (Zdiff = 100Ω)



Differential Return Loss SDD22 vs. Frequency (Zdiff = 100Ω)

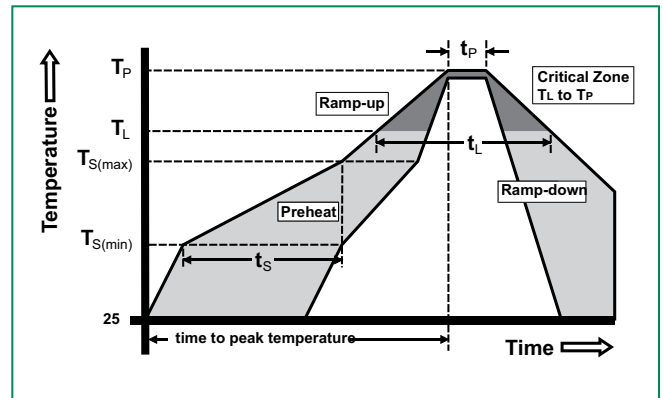


Transmission Line Pulsing (TLP) Plot



Soldering Parameters

Reflow Condition	Pb – Free assembly	
Pre Heat	- Temperature Min ($T_{s(min)}$)	150°C
	- Temperature Max ($T_{s(max)}$)	200°C
	- Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{s(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	- Temperature (T_L) (Liquidus)	217°C
	- Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_p)		260 ^{+0/-5} °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_p)		8 minutes Max.
Do not exceed		260°C



Product Characteristics

Lead Plating	Pre-Plated Frame
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Substrate material	Silicon
Body Material	V-0 per UL 94 Molded Epoxy

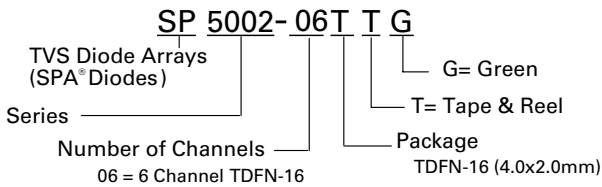
Notes :

1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
5. Package surface matte finish VDI 11-13.

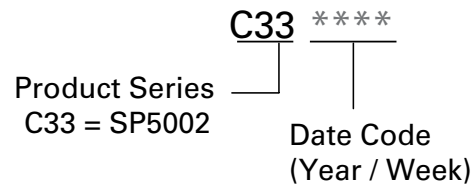
Ordering Information

Part Number	Package	Size	Marking	Min. Order Qty.
SP5002-06TTG	TDFN-16	4.0x2.0mm	C33****	3000

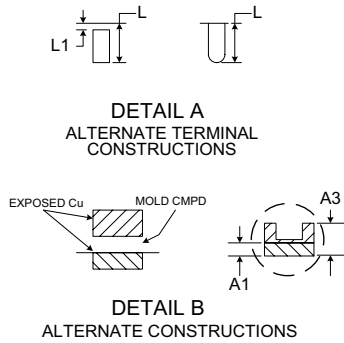
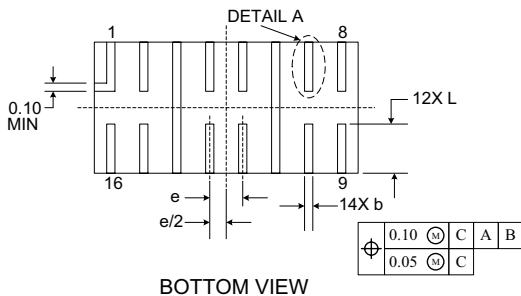
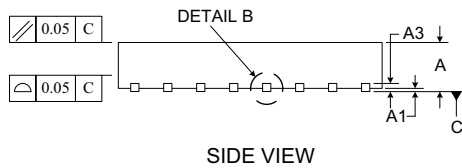
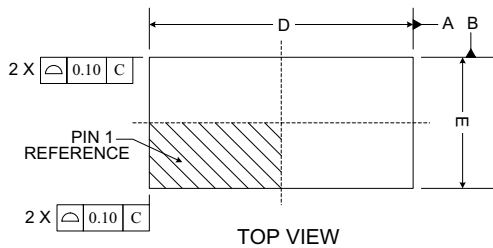
Part Numbering System



Part Marking System



Package Dimensions – TDFN-16



	TDFN-16			
	JEDEC MO-229			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.00	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	4.00 BSC		0.157 BSC	
E	2.00 BSC		0.079 BSC	
e	0.50 BSC		0.020 BSC	
L	0.70	0.90	0.028	0.035
L1	0.05	0.15	0.002	0.006

