BITSTREAM CONVERSION

UDA1338H

Multichannel audio coder-decoder

Rev. 04 — 18 May 2010 **Product data sheet**

1. General description

The UDA1338H is a single-chip consisting of 4 plus 1 analog-to-digital converters and 6 digital-to-analog converters with signal processing features employing bitstream conversion techniques. The multichannel configuration makes the device eminently suitable for use in digital audio equipment which incorporates surround feature.

The UDA1338H supports conventional 2 channels per line data transfer conformable to the I^2S-bus format with word lengths of up to 24 bits, the MSB-justified format with word lengths of up to 24 bits and the LSB-justified format with word lengths of 16 bits, 20 bits and 24 bits, as well as 4 to 6 channels per line transfer mode. The device also supports a combination of the MSB-justified output format and the LSB-justified input format. The UDA1338H has special sound processing features in the Direct Stream Digital (DSD) playback mode, de-emphasis, volume and mute which can be controlled via the L3-bus or I^2C-bus interface.

2. Features and benefits

2.1 General

- 2.7 V to 3.6 V power supply
- 5 V tolerant digital inputs
- 24-bit data path
- Selectable control: via L3-bus or I^2C-bus microcontroller interface
- Supports sample frequency ranges for:
  - Audio ADC: f_s = 16 kHz to 100 kHz
  - Voice ADC: f_s = 7 kHz to 50 kHz
  - Audio DAC: f_s = 16 kHz to 200 kHz
- Separate power control for ADC and DAC
- ADC plus integrated high-pass filter to cancel DC offset
- Integrated digital filter plus DAC
- Slave mode only applications
- Easy application

2.2 Multiple format data interface

- Audio interface supports standard I^2S-bus, MSB-justified, LSB-justified and two multichannel formats
- Voice interface supports I^2S-bus and mono channel formats

2.3 Digital sound processing

- Control via L3-bus or I^2C-bus:
  - Channel independent digital logarithmic volume
  - Digital de-emphasis for f_s = 32 kHz, 44.1 kHz, 48 kHz or 96 kHz
  - Soft or quick mute
  - Output signal polarity control

2.4 Advanced audio configuration

- Inputs:
  - 4 single-ended audio inputs (2 × stereo) with programmable gain amplifiers
  - 1 single-ended voice input
- Outputs:
  - 6 differential audio outputs (3 × stereo)
- DSD mode to support stereo DSD playback
- High linearity, wide dynamic range and low distortion
- DAC digital filter with selectable sharp or soft roll-off

3. Applications

- Excellently suitable for multichannel home audio-video application

4. Quick reference data

Table 1: Quick reference data

$V_{DDD} = V_{DDA(AD)} = V_{DDA(DA)}$ = 3.3 V; T_{amb} = 25 °C; R_L = 22 kΩ; all voltages referenced to ground (pins V_{SS}); unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supplies						
$V_{DDA(AD)}$	ADC analog supply voltage		2.7	3.3	3.6	V
$V_{DDA(DA)}$	DAC analog supply voltage		2.7	3.3	3.6	V
V_{DDD}	digital supply voltage		2.7	3.3	3.6	V
$I_{DDA(AD)}$	ADC analog supply current	f_{ADC} = 48 kHz	-	30	-	mA
$I_{DDA(DA)}$	DAC analog supply current	f_{DAC} = 48 kHz	-	20	-	mA
I_{DDD}	digital supply current	$f_{ADC} = f_{DAC}$ = 48 kHz; f_{VOICE} = 48 kHz	-	31	-	mA

Table 1: Quick reference data *...continued*

$V_{DDD} = V_{DDA(AD)} = V_{DDA(DA)} = 3.3$ V; $T_{amb} = 25$ °C; $R_L = 22$ kΩ; all voltages referenced to ground (pins V_{SS}); unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
$I_{DDD(pd)}$	digital supply current in Power-down mode	audio and voice ADCs power-down		-	18	-	mA
		DAC power-down		-	14	-	mA
T_{amb}	ambient temperature			−20	-	+85	°C
Audio analog-to-digital converter							
D_0	digital output level	at 0 dB setting; 900 mV (RMS) input	[1][2]	−2.5	−1.2	−0.7	dB
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	at −1 dBFS		-	−90	−83	dB
		at −60 dBFS; A-weighted		-	−40	−34	dB
S/N	signal-to-noise ratio	code = 0; A-weighted		94	100	-	dB
α_{cs}	channel separation			-	100	-	dB
Digital-to-analog converter							
Differential mode							
$V_{o(rms)}$	output voltage (RMS value)	at 0 dBFS digital input		1.9	2.0	2.1	V
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dBFS		-	−100	−93	dB
		at −60 dBFS; A-weighted		-	−50	−45	dB
S/N	signal-to-noise ratio	code = 0; A-weighted		107	114	-	dB
α_{cs}	channel separation			-	117	-	dB
Single-ended mode							
$V_{o(rms)}$	output voltage (RMS value)	at 0 dBFS digital input		-	1.0	-	V
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dBFS		-	−90	-	dB
		at −60 dBFS; A-weighted		-	−45	-	dB
S/N	signal-to-noise ratio	code = 0; A-weighted		-	110	-	dB
α_{cs}	channel separation			-	114	-	dB

[1] The input voltage can be up to 2 V (RMS) when the current through the ADC input pin is limited to approximately 1 mA by using a series resistor.

[2] The input voltage to the ADC scales proportionally with the power supply voltage.

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
UDA1338H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

6. Block diagram

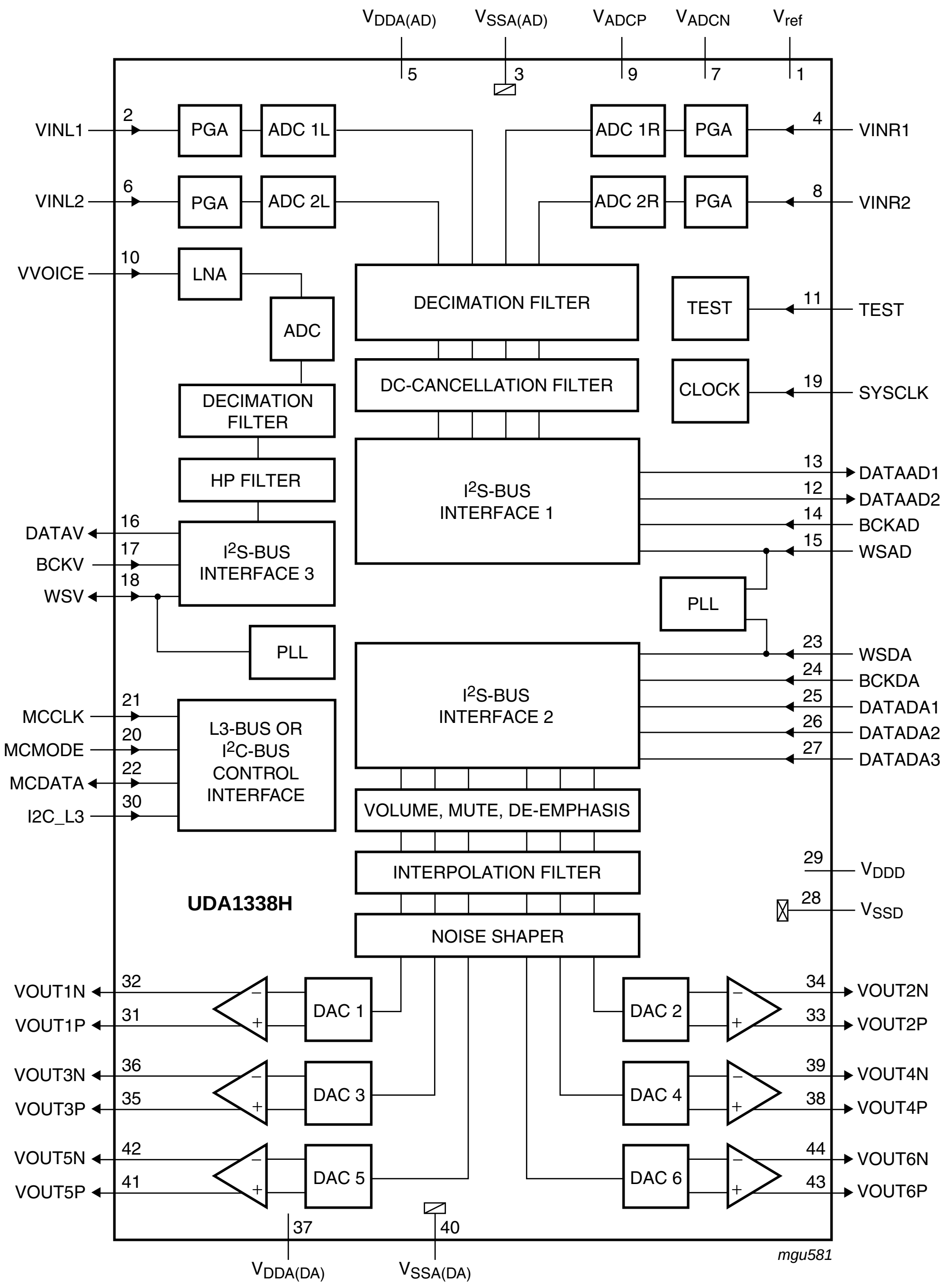


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

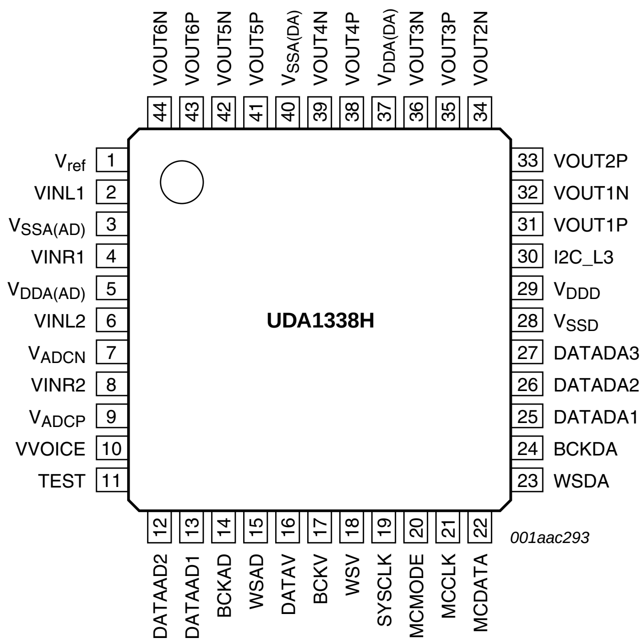


Fig 2. Pin configuration

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Type[1]	Description
V_{ref}	1	AIO	ADC reference voltage
VINL1	2	AIO	ADC 1 input left
$V_{SSA(AD)}$	3	AGND	ADC analog ground
VINR1	4	AIO	ADC 1 input right
$V_{DDA(AD)}$	5	AS	ADC analog supply voltage
VINL2	6	AIO	ADC 2 input left
V_{ADCN}	7	AIO	ADC reference voltage N
VINR2	8	AIO	ADC 2 input right
V_{ADCP}	9	AIO	ADC reference voltage P
VVOICE	10	AIO	voice ADC input
TEST	11	DID	test input; must be connected to digital ground (V_{SSD}) in application
DATAAD2	12	DO	ADC 2 data output
DATAAD1	13	DO	ADC 1 data output
BCKAD	14	DIS	ADC bit clock input
WSAD	15	DI	ADC word select input

Table 3: Pin description *...continued*

Symbol	Pin	Type[1]	Description
DATAV	16	DO	voice data output
BCKV	17	DIS	voice bit clock input
WSV	18	DIO	voice word select input or output
SYSCLK	19	DIS	system clock input: $256f_s$, $384f_s$, $512f_s$ or $768f_s$
MCMODE	20	DI	L3-bus L3MODE input or I^2C-bus DAC mute control input
MCCLK	21	DIS	L3-bus L3CLOCK input or I^2C-bus SCL input
MCDATA	22	IIC	L3-bus L3DATA input and output or I^2C-bus SDA input and output
WSDA	23	DI	DAC word select input
BCKDA	24	DIS	DAC bit clock input
DATADA1	25	DI	DAC channel 1 and channel 2 data input
DATADA2	26	DI	DAC channel 3 and channel 4 data input
DATADA3	27	DI	DAC channel 5 and channel 6 data input
V_{SSD}	28	DGND	digital ground
V_{DDD}	29	DS	digital supply voltage
I2C_L3	30	DI	selection input for L3-bus or I^2C-bus control
VOUT1P	31	AIO	DAC 1 positive output
VOUT1N	32	AIO	DAC 1 negative output
VOUT2P	33	AIO	DAC 2 positive output
VOUT2N	34	AIO	DAC 2 negative output
VOUT3P	35	AIO	DAC 3 positive output
VOUT3N	36	AIO	DAC 3 negative output
$V_{DDA(DA)}$	37	AS	DAC analog supply voltage
VOUT4P	38	AIO	DAC 4 positive output
VOUT4N	39	AIO	DAC 4 negative output
$V_{SSA(DA)}$	40	AGND	DAC analog ground
VOUT5P	41	AIO	DAC 5 positive output
VOUT5N	42	AIO	DAC 5 negative output
VOUT6P	43	AIO	DAC 6 positive output
VOUT6N	44	AIO	DAC 6 negative output

[1] See Table 4.

Table 4: Pin types

Type	Description
AGND	analog ground
AIO	analog input and output
AS	analog supply
DGND	digital ground
DI	digital input
DID	digital input with internal pull-down resistor
DIO	digital input and output

Table 4: Pin types *...continued*

Type	Description
DIS	digital Schmitt-triggered input
DO	digital output
DS	digital supply
IIC	input and open-drain output for I^2C-bus

8. Functional description

8.1 System clock

The UDA1338H operates in slave mode only; this means that in all applications the system must provide either the system clock (the bit clock for the voice ADC) or the word clock.

The audio ADC part, the voice ADC part and the DAC part can operate at different sampling frequencies (DAC-WS and ADC-WS modes) as well as a common frequency (SYSCLK, WSDA and DSD modes).

The voice ADC part supports a sampling frequency up to 50 kHz and the audio ADC supports a sampling frequency up to 100 kHz. The DAC sampling frequency range is extended up to 200 kHz with the range above 100 kHz being supported through 192 kHz sampling mode, which halves the oversampling ratio of SYSCLK and internal clocks.

The mode of operation of the audio and voice channels can be set via the L3-bus or I^2C-bus microcontroller interface and are summarized in and Table 6.

When applied, the system clock must be locked in frequency to the corresponding digital interface clocks.

The voice ADC part can either receive or generate the WSV signal as shown in Table 6.

Table 5: Audio ADC and DAC operating clock mode

Mode	Audio ADC		Audio DAC	
	Clock	Frequency	Clock	Frequency
SYSCLK	SYSCLK	$256f_s$, $384f_s$, $512f_s$ or $768f_s$	SYSCLK	$256f_s$, $384f_s$, $512f_s$ or $768f_s$
			SYSCLK	$128f_s$, $192f_s$, $256f_s$ or $384f_s$; 192 kHz sampling mode
DAC-WS	SYSCLK	$256f_s$, $384f_s$, $512f_s$ or $768f_s$	WSDA	$1f_s$
ADC-WS	WSAD	$1f_s$	SYSCLK	$256f_s$, $384f_s$, $512f_s$ or $768f_s$
			SYSCLK	$128f_s$, $192f_s$, $256f_s$ or $384f_s$; 192 kHz sampling mode
WSDA	WSDA	$1f_s$	WSDA	$1f_s$
DSD	SYSCLK	44.1 kHz × 512	SYSCLK	44.1 kHz × 512

Table 6: Voice ADC operating clock mode

Mode	Voice ADC	
	Bit clock frequency (BCKV)	Word select (WSV)
WSV-in	input: $32f_s$, $64f_s$, $128f_s$ or $256f_s$	input
WSV-out	input: $32f_s$, $64f_s$, $128f_s$ or $256f_s$	output

8.2 Audio analog-to-digital converter (audio ADC)

The audio analog-to-digital front-end of the UDA1338H consists of 4-channel single-ended Adds with programmable gain stage (from 0 dB to 24 dB with 3 dB steps), controlled via the microcontroller interface. Using the PGA feature, it is possible to accept an input signal of 900 mV (RMS) or 1.8 V (RMS) if an external resistor of 10 kΩ is used in series. The schematic of audio ADC front-end is shown in Figure 3.

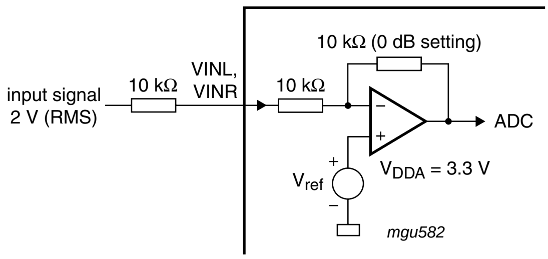


Fig 3. Schematic of audio ADC front-end

8.3 Voice analog-to-digital converter (voice ADC)

The voice analog-to-digital front-end of the UDA1338H consists of a single-channel single-ended ADC with a fixed gain (26 dB) Low Noise Amplifier (LNA). Together with the digital variable gain amplification stage, the voice ADC provides optimal processing and reproduction of the microphone signal. The supported sampling frequency range is from 7 kHz to 50 kHz. Power-down of the LNA and the ADC can be controlled separately.

8.4 Decimation filter of audio ADC

The decimation from $64f_s$ is performed in two stages. The first stage realizes $\left(\frac{\sin x}{x}\right)^4$ characteristics with a decimation factor of 8. The second stage consists of three half-band filters, each decimating by a factor of 2. The filter characteristics are shown in Table 7.

Table 7: Decimation filter characteristics (audio ADC)

Item	Condition	Value (dB)
Pass-band ripple	0 to $0.45f_s$	±0.01
Pass-band droop	$0.45f_s$	–0.2
Stop band	$>0.55f_s$	–70
Dynamic range	0 to $0.45f_s$	>135

8.5 Decimation filter of voice ADC

The voice ADC decimation filter is realized with the combination of a Finite Impulse Response (FIR) filter and Infinite Impulse Response (IIR) filter for shorter group delay. The filter characteristics are shown in Table 8. During the power-on sequence, the output of the ADC is hard muted for a certain period. This hard-mute time can be chosen between 1024 and 2048 samples.

Table 8: Decimation filter characteristics (voice ADC)

Item	Condition	Value (dB)
Pass-band ripple	0 to 0.45f_s	±0.05
Pass-band droop	0.45f_s	–0.2
Stop band	>0.55f_s	–65
Dynamic range	0 to 0.45f_s	>110

8.6 Interpolation filter of DAC

The digital interpolation filter interpolates from 1f_s to 128f_s (or to 64f_s in the 192 kHz sampling mode) by cascading FIR filters, and has two sets of filter coefficients for sharp and slow roll-off as given in Table 9 and Table 10.

Table 9: Interpolation filter characteristics (sharp roll-off)

Item	Condition	Value (dB)
Pass-band ripple	0 to 0.45f_s	±0.002
Stop band	> 0.55f_s	–75
Dynamic range	0 to 0.45f_s	> 135

Table 10: Interpolation filter characteristics (slow roll-off)

Item	Condition	Value (dB)
Pass-band ripple	0 to 0.22f_s	±0.002
Pass-band droop	0.45f_s	–3.1
Stop band	> 0.78f_s	–94
Dynamic range	0 to 0.22f_s	> 135

8.7 Noise shaper of DAC

The 3rd-order noise shaper operates at either 128f_s or 64f_s (in the 192 kHz sampling mode), and converts the 24-bit input signal into a 5-bit signal stream. The noise shaper shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved.

8.8 Digital mixer

The UDA1338H has 6 digital mixers inside the interpolator; see Figure 4. The ADC signals can be mixed with the I^2S-bus input signals. The mixing of the ADC signals can be selected by the bits MIX[1:0].

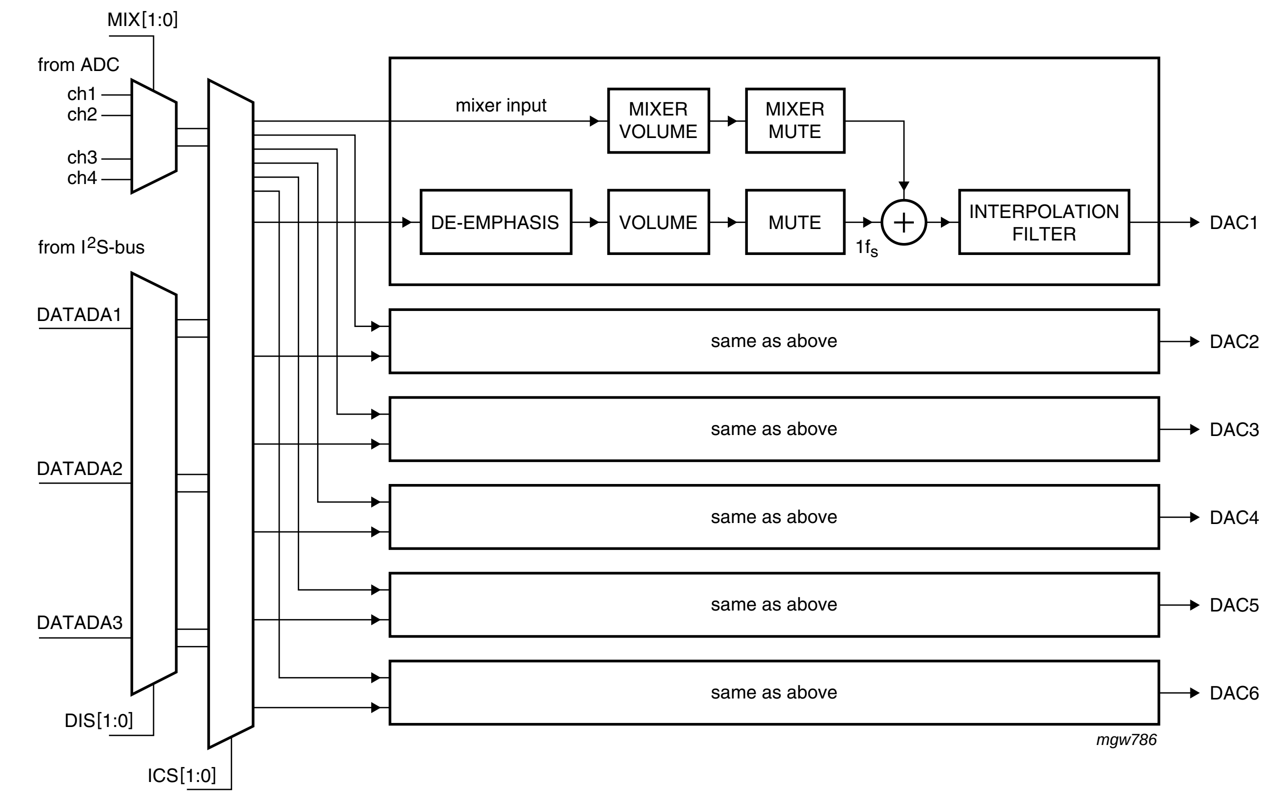


Fig 4. Block diagram of DAC mixer

8.9 Audio digital-to-analog converters

The audio digital-to-analog front-end of the UDA1338H consists of 6-channel differential SDACs: an SDAC is a multi-bit DAC based upon switched resistors. To minimize data dependent modulation effects, a Dynamic Element Matching (DEM) algorithm scrambler circuit and DC current compensation circuit are implemented with the SDAC.

8.10 Power-on reset

The UDA1338H has an internal power-on reset circuit which initializes the device; see Figure 5. All the digital sound processing features and the system controlling features are set to their default values in the L3-bus and the I^{2}C-bus modes.

The reset time (see Figure 6) is determined by an external capacitor which is connected between pin V_{ref} and ground. The reset time should be at least 250 μs for V_{ref} < 1.25 V. When $V_{DDA(AD)}$ is switched off, the device will be reset again for V_{ref} < 0.75 V.

During the reset time, the system clock should be running.

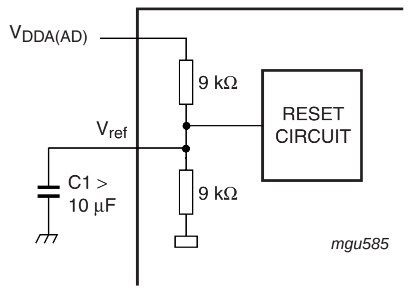


Fig 5. Power-on reset circuit

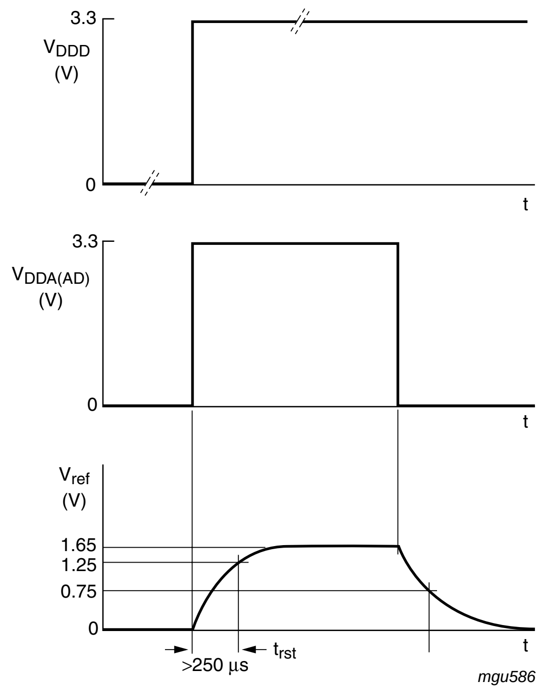


Fig 6. Power-on reset timing

8.11 Audio digital interface

The following audio formats can be selected via the microcontroller interface:

- I^{2}S-bus format with data word length of up to 24 bits
- MSB-justified format with data word length of up to 24 bits
- LSB-justified format with data word length of 16 bits, 20 bits or 24 bits
- Multichannel formats with data word length of 20 bits or 24 bits. The used data lines are DATAAD1 and DATADA1 and the sampling frequency must be below 50 kHz

The formats are illustrated in Figure 7 and Figure 8.

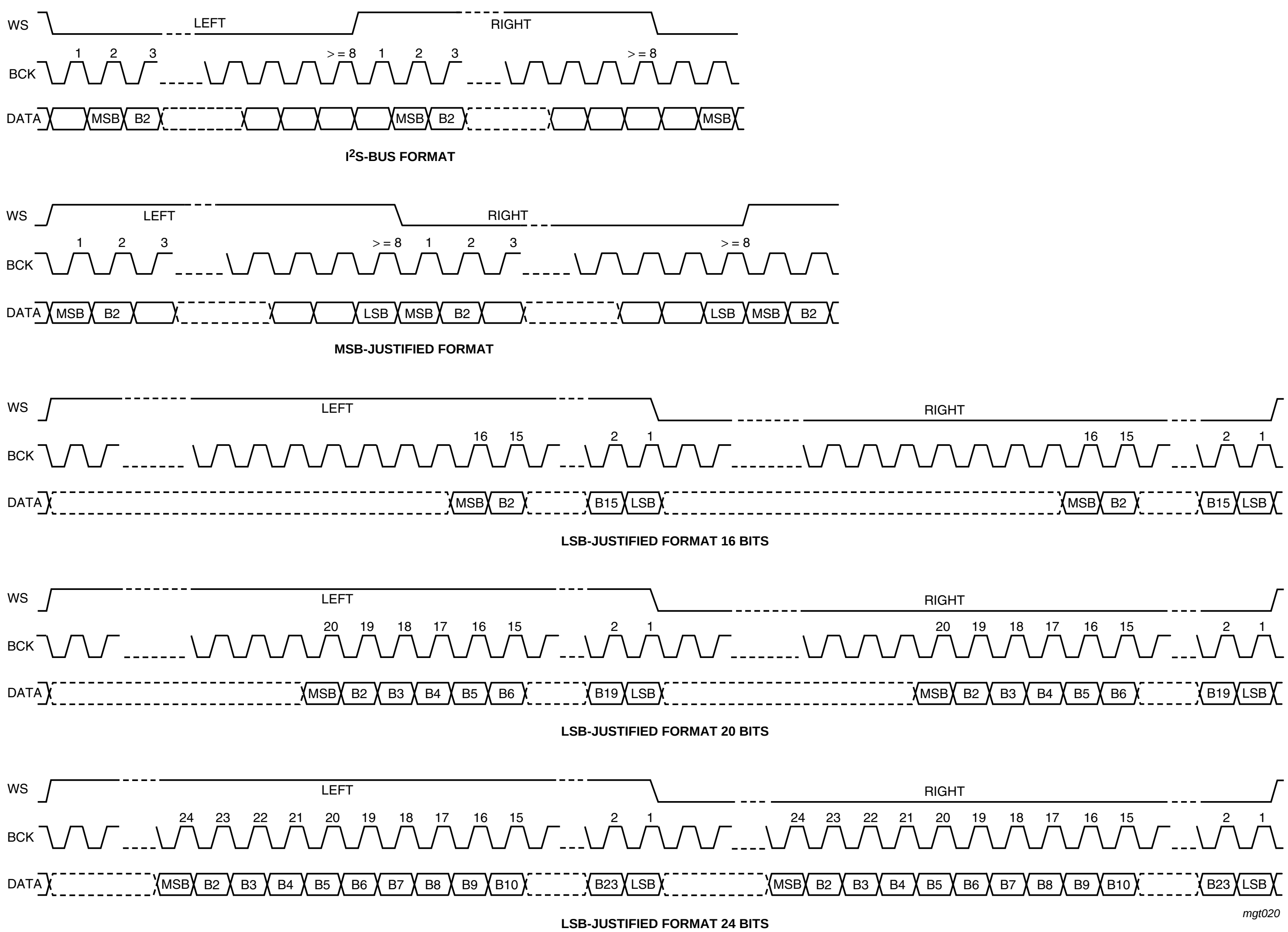
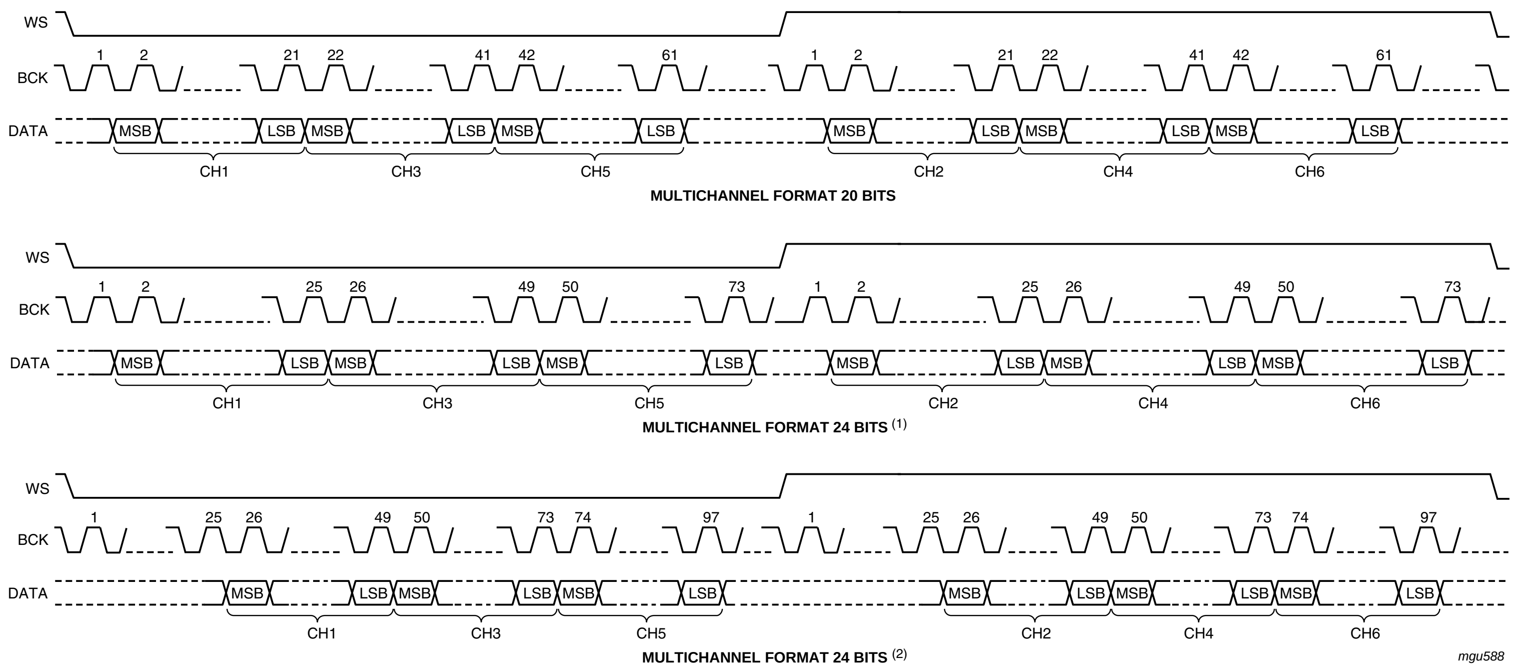


Fig 7. Formats of input and output data (single-channel)



(1) Format 1.

(2) Format 2.

Fig 8. Formats of input and output data (multichannel)

8.12 Voice digital interface

The following voice formats can be selected via the microcontroller interface:

- I²S-bus format with data word length of up to 20 bits. The left and the right channels contain the same data.
- Mono channel format with data word length of up to 20 bits

The formats are illustrated in Figure 9.

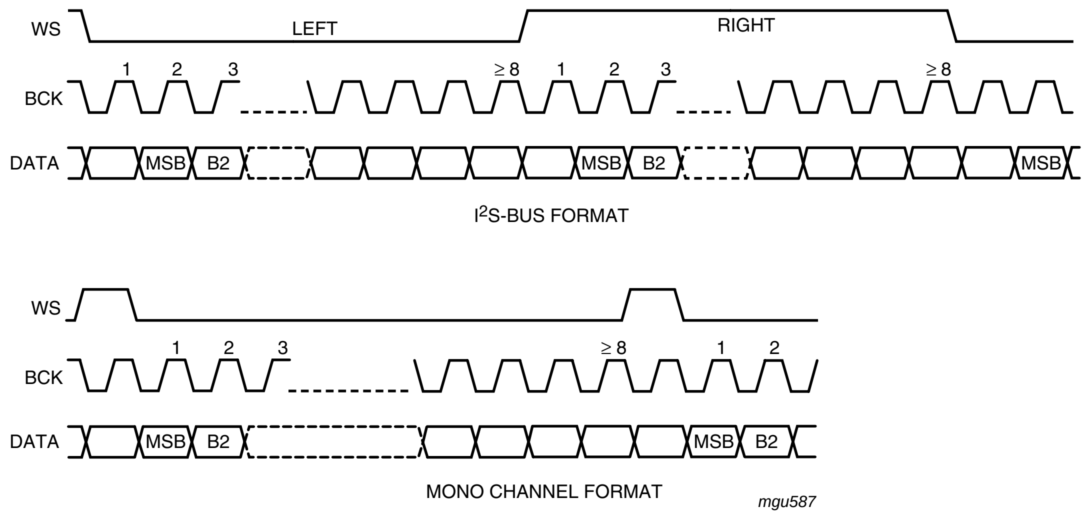


Fig 9. Voice digital interface formats

8.13 DSD mode

The UDA1338H can receive 2.8224 MHz DSD signals and generate 88.2 kHz multibit PCM signals as well as analog signal outputs. The configuration of the UDA1338H in the DSD mode is shown in Figure 10.

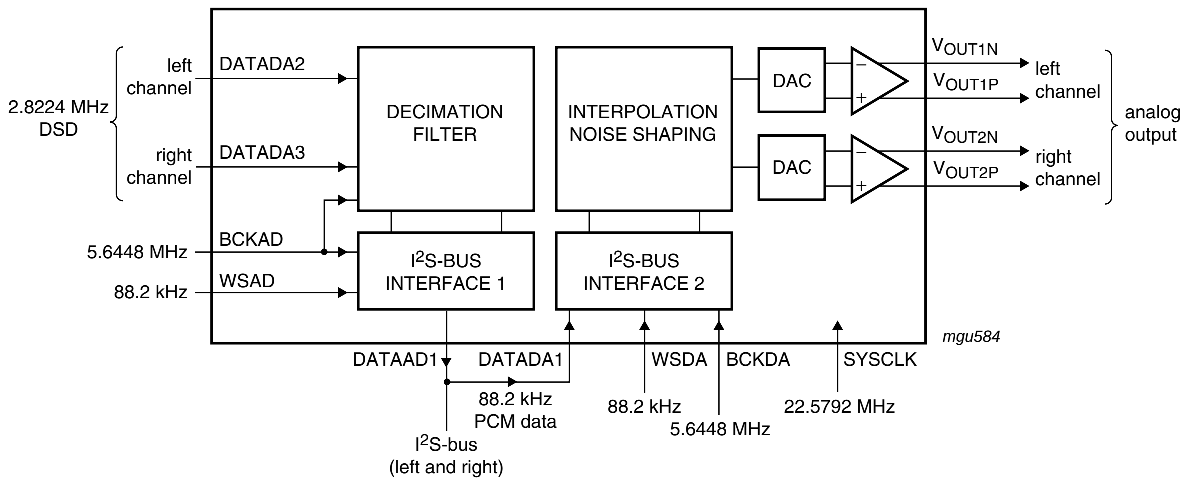


Fig 10. DSD mode

8.14 Microcontroller interface mode

The microcontroller interface mode can be selected as shown in Table 11:

- L3-bus mode when pin I2C_L3 = LOW
- I^2C-bus mode when pin I2C_L3 = HIGH

Table 11. Pin function in the L3-bus or I^2C-bus mode

Pin	Level on pin I2C_L3	
	LOW	HIGH
	L3-bus mode signal	I^2C-bus mode signal
MCCLK	L3CLOCK	SCL
MCDATA	L3DATA	SDA
MCMODE	L3MODE	QMUTE

Table 12: QMUTE

Signal QMUTE	Function
LOW	no muting
HIGH	muting

All the features are accessible with the I^2C-bus interface protocol as with the L3-bus interface protocol.

The detailed description of the device operation in the L3-bus mode and I^2C-bus mode is given in Section 9 and Section 10, respectively.

9. L3-bus interface

9.1 General

The UDA1338H has an L3-bus microcontroller interface and all the digital sound processing features and various system settings can be controlled by a microcontroller.

The exchange of data and control information between the microcontroller and the UDA1338H is LSB first and is accomplished through a serial hardware L3-bus interface comprising the following pins:

- MCCLK: clock line with signal L3CLOCK
- MCDATA: data line with signal L3DATA
- MCMODE: mode line with signal L3MODE.

The L3-bus format has two modes of operation:

- Address mode
- Data transfer mode.

The address mode is used to select a device for a subsequent data transfer. The address mode is characterized by signal L3MODE = LOW and a burst of 8 pulses for signal L3CLOCK, accompanied by 8 bits; see Figure 11.

The data transfer mode is characterized by signal L3MODE = HIGH and is used to transfer one or more bytes representing a register address, instruction or data.

Basically, two types of data transfers can be defined:

- Write action: data transfer **to** the device
- Read action: data transfer **from** the device.

9.2 Device addressing

The device address consists of one byte with:

- Data Operating Mode (DOM) bits 0 and 1 representing the type of data transfer; see Table 11.
- Address bit 2 to bit 7 representing a 6-bit device address. The address of the UDA1338H is 01 0100 (bit 2 to bit 7).

Table 13: Selection of data transfer

DOM		Transfer
Bit 0	**Bit 1**	
0	0	not used
1	0	not used
0	1	write data or prepare read
1	1	read data

9.3 Register addressing

After sending the device address (including DOM bits), indicating whether the information is to be read or written, one data byte is sent using bit 0 to indicate whether the information will be read or written and bit 1 to bit 7 for the destination register address.

Basically, there are 3 methods for register addressing:

1. Addressing for write data: bit 0 is logic 0 indicating a write action to the destination register, followed by bit 1 to bit 7 indicating the register address; see Figure 11.
2. Addressing for prepare read: bit is logic 1, indicating that data will be read from the register; see Figure 12.
3. Addressing for data read action. Here, the device returns a register address prior to sending data from that register. When bit 0 is logic 0, the register address is valid; when bit 0 is logic 1, the register address is invalid; see Figure 12.

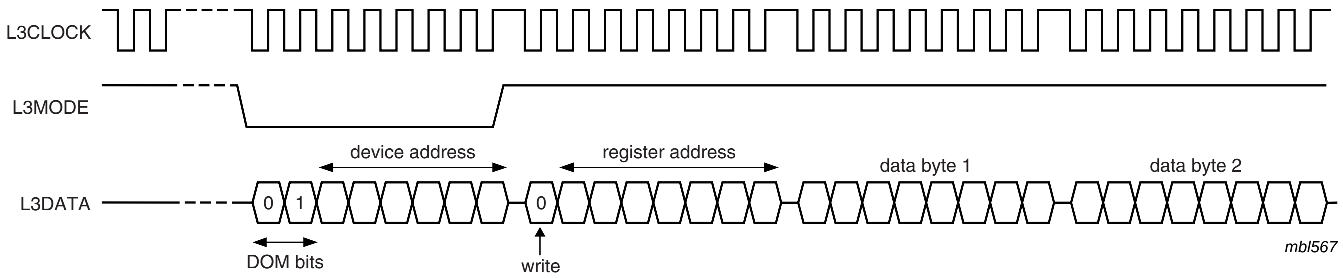


Fig 11. Data write mode

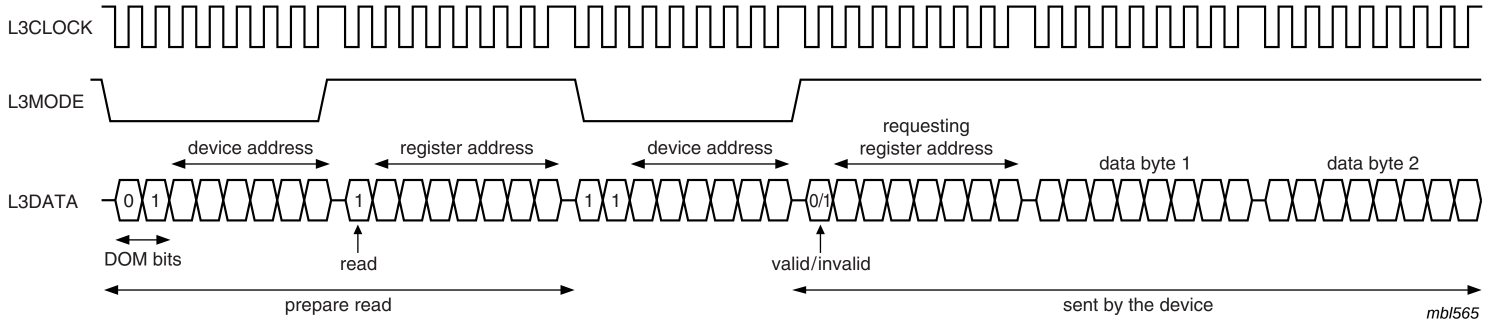


Fig 12. Data read mode

9.4 Data write mode

The data write mode is explained in the signal diagram of Figure 11. For writing data to a device, 4 bytes must be sent (see Table 14):

1. Byte 1 starting with ‘01’ for signalling the write action to the device, followed by the device address ‘01 0100’.
2. Byte 2 starting with a ‘0’ for signalling the write action, followed by 7 bits indicating the destination address in binary format with bit A6 being the MSB and bit A0 being the LSB.
3. Byte 3 with bit D15 being the MSB.
4. Byte 4 with bit D0 being the LSB.

It should be noted that each time a new destination register address needs to be written, the device address must be sent again.

9.5 Data read mode

To read data from the device, a prepare read must first be done and then data read. The data read mode is explained in the signal diagram of Figure 12.

For reading data from a device, the following 6 bytes are involved (see Table 15):

1. Byte 1 with the device address, including ‘01’ for signalling the write action to the device.
2. Byte 2 is sent with the register address from which data needs to be read. This byte starts with a ‘1’, which indicates that there will be a read action from the register, followed by 7 bits for the destination address in binary format, with bit A6 being the MSB and bit A0 being the LSB.
3. Byte 3 with the device address, including ‘11’ is sent to the device. The ‘11’ indicates that the device must write data to the microcontroller.
4. Byte 4 sent by the device to the bus, with the (requested) register address and a flag bit indicating whether the requested register was valid (bit is logic 0) or invalid (bit is logic 1).
5. Byte 5 sent by the device to the bus, with the data information in binary format, with bit D15 being the MSB.
6. Byte 6 sent by the device to the bus, with the data information in binary format, with bit D0 being the LSB.

Table 14: L3-bus write data

Byte	L3-bus mode	Action	First in time					Latest in time		
			Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1	address	device address	0	1	0	1	0	1	0	0
2	data transfer	register address	0	A6	A5	A4	A3	A2	A1	A0
3	data transfer	data byte 1	D15	D14	D13	D12	D11	D10	D9	D8
4	data transfer	data byte 2	D7	D6	D5	D4	D3	D2	D1	D0

Table 15: L3-bus read data

Byte	L3-bus mode	Action	First in time					Latest in time		
			Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1	address	device address	0	1	0	1	0	1	0	0
2	data transfer	register address	1	A6	A5	A4	A3	A2	A1	A0
3	address	device address	1	1	0	1	0	1	0	0
4	data transfer	register address	0 or 1	A6	A5	A4	A3	A2	A1	A0
5	data transfer	data byte 1	D15	D14	D13	D12	D11	D10	D9	D8
6	data transfer	data byte 2	D7	D6	D5	D4	D3	D2	D1	D0

10. I²C-bus interface

10.1 General

The UDA1338H has an I²C-bus microcontroller interface. All the features are accessible with the I²C-bus interface protocol. In the I²C-bus mode, the DAC mute function is accessible via pin MCMODE with signal QMUTE.

The exchange of data and control information between the microcontroller and the UDA1338H is accomplished through a serial hardware interface comprising the following pins as shown in Table 11:

- MCCLK: clock line with signal SCL
- MCDATA: data line with signal SDA.

10.2 Characteristics of the I²C-bus

The bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to the supply voltage V_{DD} via a pull-up resistor when connected to the output stages of a microcontroller. For a 400 kHz IC, the recommendation for this type of bus from Philips Semiconductors must be followed (e.g. up to loads of 200 pF on the bus a pull-up resistor can be used, between 200 pF and 400 pF a current source or switched resistor must be used). Data transfer can only be initiated when the bus is not busy.

10.3 Bit transfer

One data bit is transferred during each clock pulse; see Figure 13. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals. The maximum clock frequency is 400 kHz.

To be able to run on this high frequency, all the inputs and outputs connected to this bus must be designed for this high-speed I²C-bus according to the Philips specification.

10.4 Byte transfer

Each byte (8 bits) is transferred with the MSB first; see Table 16.

Table 16: Byte transfer

MSB	Bit number						LSB
7	6	5	4	3	2	1	0

10.5 Data transfer

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves.

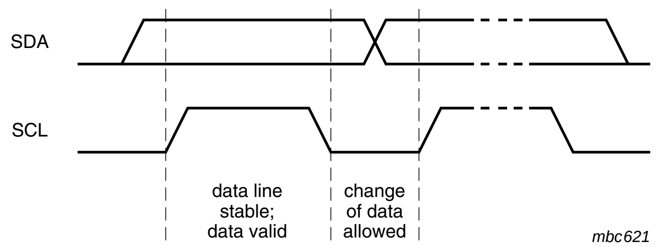


Fig 13. Bit transfer on the I²C-bus

10.6 Start and stop conditions

Both data and clock line will remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as a start condition (S); see Figure 14. A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as a stop condition (P).

10.7 Acknowledgment

The number of data bits transferred between the start and stop conditions from the transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit; see Figure 15. At the acknowledge bit the data line is released by the master and the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed, must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

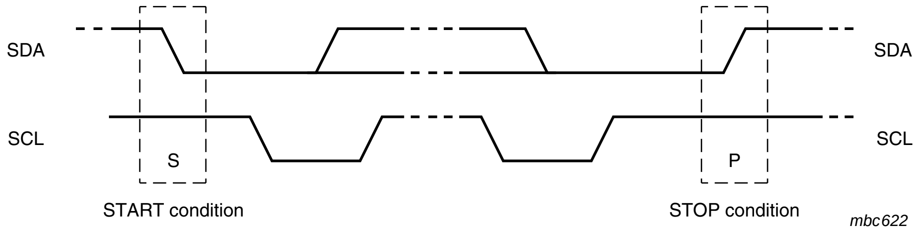


Fig 14. START and STOP conditions on the I²C-bus

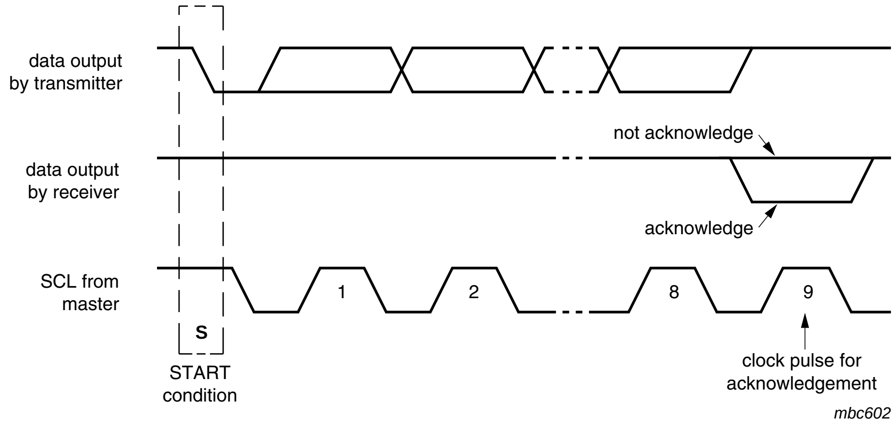


Fig 15. Acknowledge on the I²C-bus

10.8 Device address

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with byte 1 transmitted after the start procedure. The UDA1338H acts as a slave receiver or a slave transmitter.

Therefore, the clock signal SCL is only an input signal. The data signal SDA is a bidirectional line. The UDA1338H device address is shown in Table 17.

Table 17. I²C-bus device address of UDA1338H

Device address							R/$\overline{W}$
A6	A5	A4	A3	A2	A1	A0	
0	0	1	1	0	0	0	0/1

10.9 Register address

The register addresses in the I²C-bus mode are the same as in the L3-bus mode. The register addresses are defined in Section 11.

10.10 Write and read data

The I^2C-bus configurations for a write and read cycle are shown in Table 18 and Table 19, respectively.

The write cycle is used to write groups of two bytes to the internal registers for the settings. It is also possible to read the registers for the device status information.

10.11 Write cycle

The I^2C-bus configuration for a write cycle is shown in Table 18. The write cycle is used to write the data to the internal registers. The device and register addresses are one byte each, the setting data is always a pair of two bytes.

The format of the write cycle is as follows:

1. The microcontroller starts with a start condition (S).
2. The first byte (8 bits) contains the device address ‘0011 000’ and a logic 0 (write) for the R/$\overline{W}$ bit.
3. This is followed by an acknowledge (A) from the UDA1338H.
4. After this the microcontroller writes the 8-bit register address (ADDR) where the writing of the register content of the UDA1338H must start.
5. The UDA1338H acknowledges this register address (A).
6. The microcontroller sends 2 bytes data with the Most Significant (MS) byte first and then the Least Significant (LS) byte. After each byte an acknowledge is followed from the UDA1338H.
7. If repeated groups of 2 bytes data are transmitted, then the register address is auto incremented. After each byte an acknowledge is followed from the UDA1338H.
8. Finally, the UDA1338H frees the I^2C-bus and the microcontroller can generate a stop condition (P).

Table 18. Master transmitter writes to UDA1338H registers in the I^2C-bus mode

	Device address	R/$\overline{W}$		Register address		data 1				DATA 2[1]				DATA n[1]				
S	0011 000	0	A	ADDR	A	MS1	A	LS1	A	MS2	A	LS2	A	MSn	A	LSn	A	P
	acknowledge from UDA1338H																	

[1] Auto increment of register address.

10.12 Read cycle

The read cycle is used to read the data values from the internal registers. The I^2C-bus configuration for a read cycle is shown in Table 19.

The format of the read cycle is as follows:

1. The microcontroller starts with a start condition (S).
2. The first byte (8 bits) contains the device address ‘0011 000’ and a logic 0 (write) for the R/$\overline{W}$ bit.
3. This is followed by an acknowledge (A) from the UDA1338H.

4. After this the microcontroller writes the 8-bit register address (ADDR) where the reading of the register content of the UDA1338H must start.
5. The UDA1338H acknowledges this register address.
6. Then the microcontroller generates a repeated start (Sr).
7. Then the microcontroller generates the device address ‘0011 000’ again, but this time followed by a logic 1 (read) of the R/$\overline{W}$ bit. An acknowledge is followed from the UDA1338H.
8. The UDA1338H sends 2 bytes data with the Most Significant (MS) byte first and then the Least Significant (LS) byte. After each byte an acknowledge is followed from the microcontroller (master).
9. If repeated groups of 2 bytes are transmitted, then the register address is auto incremented. After each byte an acknowledge is followed from the microcontroller.
10. The microcontroller stops this cycle by generating a negative acknowledge (NA).
11. Finally, the UDA1338H frees the I^{2}C-bus and the microcontroller can generate a stop condition (P).

Table 19. Master transmitter reads from the UDA1338H registers in the I^{2}C-bus mode

	Device address	R/$\overline{W}$		Register address			Device address	R/$\overline{W}$		data 1				DATA 2[1]				DATA n[1]				
S	0011 000	0	A	ADDR	A	Sr	0011 000	1	A	MS1	A	LS1	A	MS2	A	LS2	A	MSn	A	LSn	NA	P
	acknowledge from UDA1338H									acknowledge from master												

[1] Auto increment of register address.

11. Register mapping

In this chapter the register addressing and mapping of the microcontroller interface of the UDA1338H is given.

In Table 20 an overview of the register mapping is given.

In Table 21 the actual register mapping is given and the register definitions are explained in Section 11.3 to Section 11.14.

11.1 Address mapping

Table 20: Overview of register mapping

Address	Function
System settings	
00h	system
01h	audio ADC and DAC subsystem
02h	voice ADC system
Status (read out registers)	
0Fh	status outputs
Interpolator settings	
10h	DAC channel and feature selection
11h	DAC feature control

Table 20: Overview of register mapping *…continued*

Address	Function
12h	DAC channel 1
13h	DAC channel 2
14h	DAC channel 3
15h	DAC channel 4
16h	DAC channel 5
17h	DAC channel 6
18h	DAC mixing channel 1
19h	DAC mixing channel 2
1Ah	DAC mixing channel 3
1Bh	DAC mixing channel 4
1Ch	DAC mixing channel 5
1Dh	DAC mixing channel 6
ADC input amplifier gain settings	
20h	audio ADC input amplifier gain
21h	voice ADC input amplifier gain
Supplemental settings	
30h	supplemental settings 1
31h	supplemental settings 2

11.2 Register mapping

Table 21: UDA1338H register mapping[1]

Add	Function	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
System settings																	
00h	system	RST[2]	VFS1	VFS0	VCE	VAP	DSD	SC1	SC0	OP1	OP0	FS1	FS0	ACE	ADP	DCE	DAP
		-	0	0	1	0	0	0	0	0	0	0	1	1	0	1	0
01h	audio ADC and DAC subsystem	DC	PAB	PAA	MTB	MTA	AIF2	AIF1	AIF0	DAG	FIL	DVD	DIS1	DIS0	DIF2	DIF1	DIF0
		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02h	voice ADC system	-	-	-	-	-	-	-	-	BCK1	BCK0	WSM	VH1	VH0	PVA	MTV	VIF
		0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0
Status (read out only)																	
0Fh	status outputs	-	-	-	-	-	-	-	-	-	-	VS	AS1	AS0	DS2	DS1	DS0
Interpolator settings																	
10h	DAC channel and feature selection	MIX1	MIX0	MC5	MC4	MC3	MC2	MC1	MC0	SEL1	SEL0	CS5	CS4	CS3	CS2	CS1	CS0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11h	DAC feature control	ICS1	ICS0	DE2	DE1	DE0	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12h	DAC channel 1	ICS1	ICS0	DE2	DE1	DE0	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13h	DAC channel 2	-	-	DE2	DE1	DE0	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14h	DAC channel 3	ICS1	ICS0	DE2	DE1	DE0	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15h	DAC channel 4	-	-	DE2	DE1	DE0	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16h	DAC channel 5	ICS1	ICS0	DE2	DE1	DE0	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17h	DAC channel 6	-	-	DE2	DE1	DE0	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18h	DAC mixing channel 1	ICS1	ICS0	-	-	-	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 21: UDA1338H register mapping[1] *…continued*

Add	Function	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
19h	DAC mixing channel 2	-	-	-	-	-	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1Ah	DAC mixing channel 3	ICS1	ICS0	-	-	-	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1Bh	DAC mixing channel 4	-	-	-	-	-	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1Ch	DAC mixing channel 5	ICS1	ICS0	-	-	-	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1Dh	DAC mixing channel 6	-	-	-	-	-	PD	MT	QM	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADC input amplifier gain settings																	
20h	ADC 1 and ADC 2 input amplifier gain	-	-	-	-	IB3	IB2	IB1	IB0	-	-	-	-	IA3	IA2	IA1	IA0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21h	voice ADC input amplifier gain	-	-	-	-	-	-	-	-	-	-	-	IV4	IV3	IV2	IV1	IV0
		-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0
Supplemental settings																	
30h	supplemental settings 1	-	-	-	-	-	-	-	-	PDT	-	-	-	-	-	-	-
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
31h	supplemental settings 2	-	-	-	-	-	-	-	-	-	DITH2	DITH1	DITH0	-	-	VMTP	PDLNA
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[1] When writing new settings via the L3-bus interface, the default values should always be set to warrant correct operation. Read access to the DAC features register 11h will not return valid data.

[2] When bit RST is set to logic 1, the default values are set to all the registers as shown in Table 21. When start-up, all the registers in 00h are initialized as the default values and the mute control bits MTA, MTB, MTV, MT and QM are set to logic 1. All other registers have non fixed values.

11.3 System settings

Table 22: System register (address 00h)

Bit	15	14	13	12	11	10	9	8
Symbol	RST	VFS1	VFS0	VCE	VAP	DSD	SC1	SC0
Reset default	-	0	0	1	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Symbol	OP1	OP0	FS1	FS0	ACE	ADP	DCE	DAP
Reset default	0	0	0	1	1	0	1	0

Table 23: Description of system register bits

Bit	Symbol	Description
15	RST	**Reset.** A 1-bit value to initialize the L3-bus registers with the default settings by writing bit RST = 1. If bit RST = 0, there is no reset.
14 to 13	VFS[1:0]	**Voice ADC sampling frequency.** A 2-bit value to select the voice ADC sampling frequency. Default 00; see Table 24.
12	VCE	**Voice ADC clock enable.** A 1-bit value to enable the voice ADC clock. If bit VCE = 1 (default), then the clock is enabled; if bit VCE = 0, then the clock is disabled.
11	VAP	**Voice ADC power control**. A 1-bit value to reduce the power consumption of the voice ADC. If bit VAP = 1, then the state is power-on; if bit VAP = 0 (default), then the state is power-off.
10	DSD	**DSD mode selection.** A 1-bit value to select the DSD mode. If bit DSD = 1, then the DSD mode; if bit DSD = 0 (default), then the normal mode.
9 to 8	SC[1:0]	**System clock frequency.** A 2-bit value to select the used external clock frequency. 128f_s system clock for the DAC can be used by setting bit DVD = 1. Default 00; see Table 25.
7 to 6	OP[1:0]	**Operating mode selection.** A 2-bit value to select the operation mode of the audio ADC and DAC. Default 00; see Table 26.
5 to 4	FS[1:0]	**Sampling frequency.** A 2-bit value to select the sampling frequency of the audio ADC and DAC in the WS mode. Default 01; see Table 27.
3	ACE	**ADC clock enable.** A 1-bit value to enable the audio ADC clock. If bit ACE = 1 (default), then the clock is enabled; if bit ACE = 0, then the clock is disabled.
2	ADP	**ADC power control**. A 1-bit value to reduce the power consumption of the audio ADC. If bit ADP = 1, then the state is power-on; if bit ADP = 0 (default), then the state is power-off.
1	DCE	**DAC clock enable.** A 1-bit value to enable the DAC clock. If bit DCE = 1 (default), then the clock is enabled; if bit DCE = 0, then the clock is disabled.
0	DAP	**DAC power control**. A 1-bit value to reduce the power consumption of the DAC. If bit DAP = 1, then the state is power-on; if bit DAP = 0 (default), then the state is power-off.

Table 24: Voice ADC sampling frequency bits

VFS1	VFS0	Function
0	0	6.25 kHz to 12.5 kHz (default)
0	1	12.5 kHz to 25 kHz
1	0	25 kHz to 50 kHz
1	1	reserved

Table 25: System clock frequency bits

SC1	SC0	ADC	DAC		Remark
			Bit DVD = 0	Bit DVD = 1	
0	0	$256f_s$	$256f_s$	$128f_s$	default
0	1	$384f_s$	$384f_s$	$192f_s$	
1	0	$512f_s$	$512f_s$	$256f_s$	
1	1	$768f_s$	$768f_s$	$384f_s$	

Table 26: Operating mode bits

OP1	OP0	ADC mode	DAC mode	Remark
0	0	SYSCLK ($256f_s$, $384f_s$, $512f_s$ or $768f_s$)	SYSCLK ($128f_s$, $256f_s$, $384f_s$, $512f_s$ or $768f_s$)	default
0	1	SYSCLK ($256f_s$, $384f_s$, $512f_s$ or $768f_s$)	WSDA ($1f_s$)	
1	0	WSAD ($1f_s$)	SYSCLK ($128f_s$, $256f_s$, $384f_s$, $512f_s$ or $768f_s$)	
1	1	WSDA ($1f_s$)	WSDA ($1f_s$)	

Table 27: Audio ADC and DAC sampling frequency bits

FS1	FS0	Function
0	0	12.5 kHz to 25 kHz
0	1	25 kHz to 50 kHz (default)
1	0	50 kHz to 100 kHz
1	1	100 kHz to 200 kHz

11.4 Audio ADC and DAC subsystem settings

Table 28: Audio ADC and DAC subsystem register (address 01h)

Bit	15	14	13	12	11	10	9	8
Symbol	DC	PAB	PAA	MTB	MTA	AIF2	AIF1	AIF0
Reset default	1	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Symbol	DAG	FIL	DVD	DIS1	DIS0	DIF2	DIF1	DIF0
Reset default	0	0	0	0	0	0	0	0

Table 29: Description of the audio ADC and DAC subsystem register bits

Bit	Symbol	Description
15	DC	**ADC DC-filter.** A 1-bit value to enable the digital DC-filter of the ADC. If bit DC = 1 (default), then the DC-filtering is active; if bit DC = 0, then there is no DC-filtering.
14	PAB	**Polarity ADC 2 control.** A 1-bit value to control the ADC 2 polarity. If bit PAB = 1, then the polarity is inverted; if bit PAB = 0 (default), then the polarity is non-inverted.
13	PAA	**Polarity ADC 1 control.** A 1-bit value to control the ADC 1 polarity. If bit PAA = 1, then the polarity is inverted; if bit PAA = 0 (default), then the polarity is non-inverted.
12	MTB	**Mute ADC 2.** A 1-bit value to enable the digital mute of ADC 2. If bit MTB = 1, then ADC 2 is soft muted; if bit MTB = 0 (default), then ADC 2 is not muted.
11	MTA	**Mute ADC 1.** A 1-bit value to enable the digital mute of ADC 1. If bit MTA = 1, then ADC 1 is soft muted; if bit MTA = 0 (default), then ADC 1 is not muted.
10 to 8	AIF[2:0]	**ADC output data interface format.** A 3-bit value to select the used data format to the I^2S-bus ADC output interface. Default 000; see Table 30.
7	DAG	**DAC gain switch.** A 1-bit value to select the DAC gain. If bit DAG = 1, then the gain is 6 dB; if bit DAG = 0 (default), then the gain is 0 dB.
6	FIL	**Filter selection.** A 1-bit value to select the interpolation filter characteristics. If bit FIL = 1, then slow roll-off; if bit FIL = 0 (default), then sharp roll-off.
5	DVD	**192 kHz sampling mode selection.** A 1-bit value to select the oversampling rate of the noise shaper. The $64f_s$ rate is used for 192 kHz and 176.4 kHz sampling frequencies. If 7-bit DVD = 1, then $64f_s$ rate is selected (192 kHz sampling mode); if bit DVD = 0 (default), then $128f_s$ rate is selected.
4 to 3	DIS[1:0]	**Data interface selection.** A 2-bit value to select the data interface connection. Default 00; see Table 31.
2 to 0	DIF[2:0]	**DAC input data interface format.** A 3-bit value to select the used data format to the I^2S-bus DAC input interface. Default 000; see Table 30.

Table 30: Data interface format bits

AIF2	AIF1	AIF0	Function
DIF2	DIF1	DIF0	
0	0	0	I^2S-bus format (default)
0	0	1	LSB-justified format, 16 bits
0	1	0	LSB-justified format, 20 bits
0	1	1	LSB-justified format, 24 bits
1	0	0	MSB-justified format
1	0	1	multichannel format, 20 bits
1	1	0	multichannel format, 24 bits (format 1)
1	1	1	multichannel format, 24 bits (format 2)

Table 31: Data interface selection bits

DIS1	DIS0	Input to DAC
0	0	DATADA1 to DAC channel 1 and channel 2, DATADA2 to DAC channel 3 and channel 4, and DATADA3 to DAC channel 5 and channel 6 (default)
0	1	DATADA1 to DAC channel 1 to channel 6
1	0	DATADA2 to DAC channel 1 to channel 6
1	1	DATADA3 to DAC channel 1 to channel 6

11.5 Voice ADC system settings

Table 32: Voice ADC system register (address 02h)

Bit	15	14	13	12	11	10	9	8
Symbol	-	-	-	-	-	-	-	-
Reset default	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Symbol	BCK1	BCK0	WSM	VH1	VH0	PVA	MTV	VIF
Reset default	0	1	1	0	1	0	0	0

Table 33: Description of the voice ADC system register bits

Bit	Symbol	Description
15 to 8	-	default 0000 0000
7 to 6	BCK[1:0]	**BCK frequency of voice ADC.** A 2-bit value to select the BCK frequency of the voice ADC in the WSV-out mode. Default 01; see Table 34.
5	WSM	**WSV mode selection.** A 1-bit value to select the WSV mode of the voice ADC. If bit WSM = 1 (default), then WSV-in mode; if bit WSM = 0, then WSV-out mode.
4 to 3	VH[1:0]	**Voice ADC high-pass filter setting.** A 2-bit value to enable the high-pass filter of the voice ADC. Default 01; see Table 35.
2	PVA	**Polarity voice ADC control.** A 1-bit value to control the voice ADC polarity. If bit PVA = 1, then the polarity is inverted; if bit PVA = 0 (default), then the polarity is non-inverted.
1	MTV	**Mute voice ADC.** A 1-bit value to enable the digital mute of the voice ADC. If bit MTV = 1, then the voice ADC is soft muted; if bit MTV = 0 (default), then the voice ADC is not muted.
0	VIF	**Voice ADC interface format.** A 1-bit value to select the data interface format of the voice ADC. If bit VIF = 1, then mono-channel format; if bit VIF = 0 (default), then I^2S-bus format.

Table 34: BCK frequency of voice ADC bits

BCK1	BCK0	Function
0	0	$32f_s$
0	1	$64f_s$ (default)
1	0	$128f_s$
1	1	$256f_s$

Table 35: Voice ADC high-pass filter setting bits

VH1	VH0	Function
0	0	high-pass filter off
0	1	$f_c = 0.00008f_s$ (default)
1	0	$f_c = 0.0125f_s$
1	1	$f_c = 0.025f_s$

11.6 Status output register (read only)

Table 36: Status output register (address 0Fh)

Bit	15	14	13	12	11	10	9	8
Symbol	-	-	-	-	-	-	-	-
Bit	7	6	5	4	3	2	1	0
Symbol	-	-	VS	AS1	AS0	DS2	DS1	DS0

Table 37: Description of status output register bits

Bit	Symbol	Description
15 to 6	-	not used
5	VS	**Voice ADC status.** A 1-bit value to indicate the hard mute status of the voice ADC. If bit VS = 1, then power-down is ready and the clock may be disabled; if bit VS = 0, then power-down is not ready and the clock should not be disabled.
4	AS1	**ADC 2 status.** A 1-bit value to indicate the hard mute status of ADC 2. If bit AS1 = 1, then power-down is ready and the clock may be disabled; if bit AS1 = 0, then power-down is not ready and the clock should not be disabled.
3	AS0	**ADC 1 status.** A 1-bit value to indicate the hard mute status of ADC 1. If bit AS0 = 1, then power-down is ready and the clock may be disabled; if bit AS0 = 0, then power-down is not ready and the clock should not be disabled.
2	DS2	**DAC channel 5 and channel 6 status.** A 1-bit value to indicate the hard mute status of DAC channel 5 and channel 6. If bit DS2 = 1, then power-down is ready and the clock may be disabled; if bit DS2 = 0, then power-down is not ready and the clock should not be disabled.
1	DS1	**DAC channel 3 and channel 4 status.** A 1-bit value to indicate the hard mute status of DAC channel 3 and channel 4. If bit DS1= 1, then power-down is ready and the clock may be disabled; if bit DS1 = 0, then power-down is not ready and the clock should not be disabled.
0	DS0	**DAC channel 1 and channel 2 status.** A 1-bit value to indicate the hard mute status of DAC channel 1 and channel 2. If bit DS0 = 1, then power-down is ready and the clock may be disabled; if bit DS0 = 0, then power-down is not ready and the clock should not be disabled.

11.7 DAC channel selection

Table 38: DAC channel select register (address 10h)

Bit	15	14	13	12	11	10	9	8
Symbol	MIX1	MIX0	MC5	MC4	MC3	MC2	MC1	MC0
Reset default	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Symbol	SEL1	SEL0	CS5	CS4	CS3	CS2	CS1	CS0
Reset default	0	0	0	0	0	0	0	0

Table 39: Description of DAC channel select register bits

Bit	Symbol	Description
15 to 14	MIX[1:0]	**DAC mixer setting.** A 2-bit value to enable the DAC mixer. Default 00; see Table 40.
13 to 8	MC[5:0]	**DAC mixing channel selection.** A group of 6 enable bits to make DAC mixing channels ready for receiving feature settings through register address 11H. Only selected registers accept new settings. Default 00 0000 (no channel ready); see Table 41.
7 and 6	SEL[1:0]	**Feature selection.** A 2-bit value to select the features to be set through register address 11H. When the feature settings are written, only selected feature settings are changed and non selected features are kept unchanged. Default 00; see Table 42.
5 to 0	CS[5:0]	**DAC channel selection.** A group of 6 enable bits to make DAC channel ready for receiving feature settings through register address 11H. Default 00 0000 (no channel ready); see Table 41.

Table 40: DAC mixer setting bits

MIX1	MIX0	Function
0	0	no mixing (default)
0	1	no mixing
1	0	mixing ADC 1
1	1	mixing ADC 2

Table 41: DAC channel and mixing channel selection bits

MC5	MC4	MC3	MC2	MC1	MC0	Function
CS5	CS4	CS3	CS2	CS1	CS0	
0	0	0	0	0	1	channel 1 selected
:	:	:	:	:	:	
0	0	1	0	1	0	channel 2 and channel 4 selected
:	:	:	:	:	:	
1	1	1	1	1	1	all channels selected

Table 42: Feature selection bits

SEL1	SEL0	Function
0	0	all features (default)
0	1	volume
1	0	mute and quick mute
1	1	de-emphasis, polarity and input channel selection

11.8 DAC features settings

Table 43: DAC features register (addresses 11h)

Bit	15	14	13	12	11	10	9	8
Symbol	ICS1	ICS0	DE2	DE1	DE0	PD	MT	QM
Reset default	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Symbol	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
Reset default	0	0	0	0	0	0	0	0

Table 44: Description of DAC features register bits

Bit	Symbol	Description
15 to 14	ICS[1:0]	**Input channel selection.** A 2-bit value to select the input channels. As the controlled channels are paired off, this 2-bit value must be written to each odd channel register. Default 00; see Table 45.
13 to 11	DE[2:0]	**De-emphasis setting.** A 3-bit value to enable the digital de-emphasis filter. Default 000; see Table 46.
10	PD	**Polarity DAC control.** A 1-bit value to control the DAC polarity. If bit PD = 1, then the polarity is inverted; if bit PD = 0 (default), then the polarity is non-inverted.
9	MT	**Muting.** A 1-bit value to enable the digital mute. All the DAC outputs are muted at start-up. It is necessary to explicitly switch off for the audio output by means of bit MT. If bit MT = 1 (start-up), then muting; if bit MT = 0 (default), then no muting.
8	QM	**Quick mute.** A 1-bit value to set the quick mute mode. If bit QM = 1 (start-up), then quick mute mode; if bit QM = 0 (default), then soft mute mode.
7 to 0	VC[7:0]	**Interpolator volume control.** An 8-bit value to program the volume attenuation of each channel. The range is from 0 to −53 dB in steps of 0.25 dB, from −53 dB to −80 dB in steps of 3 dB and −∞ dB. Default 0000 0000; see Table 47.

Table 45: Input channel selection bits

ICS1	ICS0	Input to DAC output
0	0	left channel input data to odd channel output; right channel input data to even channel output
0	1	left channel input data to odd and even channel outputs
1	0	right channel input data to odd and even channel outputs
1	1	left channel input data to even channel output; right channel input data to odd channel output

Table 46: De-emphasis bits

DE2	DE1	DE0	Function
0	0	0	no de-emphasis (default)
0	0	1	de-emphasis of 32 kHz
0	1	0	de-emphasis of 44.1 kHz
0	1	1	de-emphasis of 48 kHz
1	0	0	de-emphasis of 96 kHz
1	0	1	not used
1	1	0	not used
1	1	1	not used

Table 47: Interpolator volume control bits

VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	Volume (dB)
0	0	0	0	0	0	0	0	0 (default)
0	0	0	0	0	0	0	1	–0.25
0	0	0	0	0	0	1	0	–0.50
0	0	0	0	0	0	1	1	–0.75
0	0	0	0	0	1	0	0	–1.00
0	0	0	0	0	1	0	1	–1.25
:	:	:	:	:	:	:	:	:
1	1	0	1	0	1	0	0	–53
1	1	0	1	1	0	0	0	–56
1	1	0	1	1	1	0	0	–59
1	1	1	0	0	0	0	0	–62
1	1	1	0	0	1	0	0	–65
1	1	1	0	1	0	0	0	–68
1	1	1	0	1	1	0	0	–71
1	1	1	1	0	0	0	0	–74
1	1	1	1	0	1	0	0	–77
1	1	1	1	1	0	0	0	–80
1	1	1	1	1	1	0	0	–∞
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	–∞

11.9 DAC channel 1 to channel 6 settings

All the DAC features which are written in register 11h are copied into the odd channel registers.

Table 48: DAC channel 1, 3 and 5 registers (addresses 12h, 14h and 16h)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	ICS1	ICS0	DE2	DE1	DE0	PD	MT	QM
Reset default	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Symbol	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
Reset default	0	0	0	0	0	0	0	0

All the DAC features which are written in register 11h are copied into the even channel registers, except the bits ICS[1:0].

Table 49: DAC channel 2, 4 and 6 registers (addresses 13h, 15h and 17h)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	-	-	DE2	DE1	DE0	PD	MT	QM
Reset default	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Symbol	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
Reset default	0	0	0	0	0	0	0	0

11.10 DAC mixing channel settings

All the DAC features which are written in register 11h are copied into the odd mixing channel registers, except the bits DE[2:0].

Table 50: DAC mixing channel 1, 3 and 5 registers (addresses 18h, 1Ah and 1Ch)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	ICS1	ICS0	-	-	-	PD	MT	QM
Reset default	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Symbol	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
Reset default	0	0	0	0	0	0	0	0

All the DAC features which are written in register 11h are copied into the even channel registers, except the bits ICS[1:0] and DE[2:0].

Table 51: DAC mixing channel 2, 4 and 6 registers (addresses 19h, 1Bh and 1Dh)

Bit	15	14	13	12	11	10	9	8
Symbol	-	-	-	-	-	PD	MT	QM
Reset default	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Symbol	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
Reset default	0	0	0	0	0	0	0	0

11.11 Audio ADC 1 and ADC 2 input amplifier gain settings

Table 52: Audio ADC input amplifier gain register (address 20h)

Bit	15	14	13	12	11	10	9	8
Symbol	-	-	-	-	IB3	IB2	IB1	IB0
Reset default	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	IA3	IA2	IA1	IA0
Reset default	0	0	0	0	0	0	0	0

Table 53: Description of audio ADC input amplifier gain register bits

Bit	Symbol	Description
15 to 12	-	default 0000
11 to 8	IB[3:0]	**Audio ADC 2 input amplifier gain.** A 4-bit value to program the input amplifier gain in steps of 3 dB (9 settings). Default 0000; see Table 54.
7 to 4	-	default 0000
3 to 0	IA[3:0]	**Audio ADC 1 input amplifier gain.** A 4-bit value to program the input amplifier gain in steps of 3 dB (9 settings). Default 0000; see Table 54.

Table 54: Audio ADC input amplifier gain bits

IA3	IA2	IA1	IA0	Gain (dB)
IB3	**IB2**	**IB1**	**IB0**	
0	0	0	0	0 (default)
0	0	0	1	+3
0	0	1	0	+6
0	0	1	1	+9
0	1	0	0	+12
0	1	0	1	+15
0	1	1	0	+18
0	1	1	1	+21
1	0	0	0	+24

11.12 Voice ADC gain settings

Table 55: Voice ADC input amplifier gain register (address 21h)

Bit	15	14	13	12	11	10	9	8
Symbol	-	-	-	-	-	-	-	-
Reset default	-	-	-	-	-	-	-	-
Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	IV4	IV3	IV2	IV1	IV0
Reset default	0	0	0	0	0	0	0	0

Table 56: Description of voice ADC input amplifier gain register bits

Bit	Symbol	Description
15 to 8	-	not used
7 to 5	-	default 000
4 to 0	IV[4:0]	**Voice ADC input amplifier gain.** A 5-bit value to program the voice amplifier gain in steps of 1.5 dB (21 settings). Default 0 0000; see Table 57.

Table 57: Voice ADC input amplifier gain bits

IV4	IV3	IV2	IV1	IV0	Gain (dB)
0	0	0	0	0	0 (default)
0	0	0	0	1	+1.5
0	0	0	1	0	+3
0	0	0	1	1	+4.5
0	0	1	0	0	+6
0	0	1	0	1	+7.5
:	:	:	:	:	:
1	0	0	1	1	+28.5
1	0	1	0	0	+30
:	:	:	:	:	not used
1	1	1	1	1	not used

11.13 Supplemental settings 1

Table 58: Supplemental settings 1 register (address 30h)

Bit	15	14	13	12	11	10	9	8
Symbol	-	-	-	-	-	-	-	-
Reset default	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Symbol	PDT	-	-	-	-	-	-	-
Reset default	0	0	0	0	0	0	0	0

Table 59: Description of supplemental settings 1 register bits

Bit	Symbol	Description
15 to 8	-	default 0000 0000
7	PDT	**Power-down time.** A 1-bit value to select the time of the SDAC power-down sequence. If bit PDT = 1, then 1024/f_s seconds; if bit PDT = 0 (default), then 512/f_s seconds.
6 to 0	-	default 000 0000

11.14 Supplemental settings 2

Table 60: Supplemental settings 2 register (address 31h)

Bit	15	14	13	12	11	10	9	8
Symbol	-	-	-	-	-	-	-	-
Reset default	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Symbol	-	DITH2	DITH1	DITH0	-	-	VMTP	PDLNA
Reset default	0	0	0	0	0	0	0	0

Table 61: Description of supplemental settings 2 register bits

Bit	Symbol	Description
15 to 7	-	default 0000 0000 0
6 to 4	DITH[2:0]	**DAC dither control.** A 3-bit value to control the dithering of the SDAC. Default 000; see Table 62.
3 to 2	-	default 00
1	VMTP	**Voice mute period control.** A 1-bit value to select the voice ADC mute period at power-up. If bit VMTP = 1, then mute for 1024 samples (1024/f_s); if bit VMTP = 0 (default), then mute for 2048 samples (2048/f_s).
0	PDLNA	**Power-down voice LNA.** A 1-bit value to power-down the voice ADC LNA. It should be noted that disabling the LNA requires a recovery time defined by the external RC circuit. If bit PDNLA = 1, then power-down; if bit PDNLA = 0 (default), then power-on.

Table 62: DAC dither control bits

DITH2	DITH1	DITH0	Function
0	0	0	DC dither (MID-level); default
0	0	1	reserved
0	1	0	reserved
0	1	1	reserved
1	0	0	DC dither (LOW-level)
1	0	1	DC plus AC dither (LOW-level)
1	1	0	DC dither (HIGH-level)
1	1	1	DC plus AC dither (HIGH-level)

12. Limiting values

Table 63: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min.	Max.	Unit
V_{DD}	supply voltage		[1]	-	4.0	V
$T_{xtal(max)}$	maximum crystal temperature			-	150	°C
T_{stg}	storage temperature			−65	+125	°C
T_{amb}	operating ambient temperature			−20	+85	°C
V_{esd}	electrostatic discharge voltage		[2]	−2000	+2000	V
			[3]	−200	+200	V

[1] All supply connections must be made to the same power supply.

[2] Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.

[3] Equivalent to discharging a 200 pF capacitor via a 0.75 μH series inductor.

13. Thermal characteristics

Table 64: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	85	K/W

14. Static characteristics

Table 65: DC characteristics

V_{DDD} = $V_{DDA(AD)}$ = $V_{DDA(DA)}$ = 3.3 V; T_{amb} = 25 °C; R_L = 22 kΩ; all voltages referenced to ground (pins V_{SS}); unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Supplies							
$V_{DDA(AD)}$	ADC analog supply voltage		[1]	2.7	3.3	3.6	V
$V_{DDA(DA)}$	DAC analog supply voltage		[1]	2.7	3.3	3.6	V
V_{DDD}	digital supply voltage		[1]	2.7	3.3	3.6	V
$I_{DDA(AD)}$	ADC analog supply current	f_{ADC} = 48 kHz		-	30	-	mA
		f_{ADC} = 96 kHz		-	31	-	mA
$I_{DDA(DA)}$	DAC analog supply current	f_{DAC} = 48 kHz		-	20	-	mA
		f_{DAC} = 96 kHz		-	32	-	mA
I_{DDD}	digital supply current	f_{ADC} = f_{DAC} = 48 kHz; f_{VOICE} = 48 kHz		-	31	-	mA
		f_{ADC} = f_{DAC} = 96 kHz; f_{VOICE} = 48 kHz		-	55	-	mA
$I_{DDD(pd)}$	digital supply current in Power-down mode	audio and voice ADCs power-down		-	18	-	mA
		DAC power-down		-	14	-	mA
Digital input pins (5 V tolerant TTL compatible)							
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
I_{LI}	input leakage current			-	-	1	µA
C_i	input capacitance			-	-	10	pF
Digital output pins							
V_{OH}	HIGH-level output voltage	I_{OH} = −2 mA		0.85V_{DDD}	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA		-	-	0.4	V
Analog-to-digital converter							
V_{ref}	reference voltage on pin V_{ref}	with respect to $V_{SSA(AD)}$		0.45$V_{DDA(AD)}$	0.5$V_{DDA(AD)}$	0.55$V_{DDA(AD)}$	V
V_{ADCP}	positive reference voltage of ADC			-	$V_{DDA(AD)}$	-	V
V_{ADCN}	negative reference voltage of ADC			0.0	0.0	0.0	V
R_o	output resistance on pin V_{ref}			-	5	-	kΩ
$R_{i(ADC)}$	input resistance of audio ADC			-	10	-	kΩ

Table 65: DC characteristics *...continued*

V_{DDD} = $V_{DDA(AD)}$ = $V_{DDA(DA)}$ = 3.3 V; T_{amb} = 25 °C; R_L = 22 kΩ; all voltages referenced to ground (pins V_{SS}); unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$R_{i(VADC)}$	input resistance of voice ADC		-	5	-	kΩ
Digital-to-analog converter						
R_L	load resistance		4	-	-	kΩ
R_o	output resistance		-	1	-	kΩ

[1] All supply connections must be made to the same power supply unit.

15. Dynamic characteristics

Table 66: AC characteristics

V_{DDD} = $V_{DDA(AD)}$ = $V_{DDA(DA)}$ = 3.3 V; f_i = 1 kHz; T_{amb} = 25 °C; R_L = 22 kΩ; sampling frequency f_s = 48 kHz; all voltages referenced to ground (pins V_{SS}); unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Audio analog-to-digital converter						
D_0	digital output level	at 0 dB setting; 900 mV input [1][2]	−2.5	−1.2	−0.7	dB
		at 3 dB setting; 637 mV input [2]	-	−1.2	-	dB
		at 6 dB setting; 451 mV input [2]	-	−1.2	-	dB
		at 9 dB setting; 319 mV input [2]	-	−1.2	-	dB
		at 12 dB setting; 226 mV input [2]	-	−1.2	-	dB
		at 15 dB setting; 160 mV input [2]	-	−1.2	-	dB
		at 18 dB setting; 113 mV input [2]	-	−1.2	-	dB
		at 21 dB setting; 80 mV input [2]	-	−1.2	-	dB
		at 24 dB setting; 57 mV input [2]	-	−1.2	-	dB
ΔV_i	input voltage unbalance between channels		-	0.1	-	dB

Table 66: AC characteristics *...continued*

$V_{DDD} = V_{DDA(AD)} = V_{DDA(DA)} = 3.3$ V; $f_i = 1$ kHz; $T_{amb} = 25$ °C; $R_L = 22$ kΩ; sampling frequency $f_s = 48$ kHz; all voltages referenced to ground (pins V_{SS}); unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	normal mode; at −1 dBFS				
		at 0 dB setting	-	−90	−83	dB
		at 3 dB setting	-	−90	-	dB
		at 6 dB setting	-	−90	-	dB
		at 9 dB setting	-	−90	-	dB
		at 12 dB setting	-	−90	-	dB
		at 15 dB setting	-	−89	-	dB
		at 18 dB setting	-	−87	-	dB
		at 21 dB setting	-	−85	-	dB
		at 24 dB setting	-	−83	-	dB
		normal mode; at −60 dBFS; A-weighted				
		at 0 dB setting	-	−40	−34	dB
		at 3 dB setting	-	−40	-	dB
		at 6 dB setting	-	−40	-	dB
		at 9 dB setting	-	−39	-	dB
		at 12 dB setting	-	−38	-	dB
		at 15 dB setting	-	−37	-	dB
		at 18 dB setting	-	−35	-	dB
		at 21 dB setting	-	−32	-	dB
		at 24 dB setting	-	−30	-	dB
S/N	signal-to-noise ratio	code = 0; A-weighted	94	100	-	dB
α_{cs}	channel separation		-	100	-	dB
Voice analog-to-digital converter						
$V_{i(rms)}$	input voltage (RMS value)	at 0 dBFS digital output; 2.2 kΩ source impedance	-	50.0	-	mV
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	at −1 dBFS	-	−78	-	dB
		at −20 dBFS	-	−65	-	dB
		at −40 dBFS; A-weighted	-	−47	-	dB
S/N	signal-to-noise ratio	code = 0; A-weighted	-	87	-	dB
Digital-to-analog converter						
Differential mode						
$V_{o(rms)}$	output voltage (RMS value)	at 0 dBFS digital input	1.9	2.0	2.1	V
ΔV_o	output voltage unbalance between channels		-	<0.1	-	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dBFS	-	−100	−93	dB
		at −20 dBFS	-	−90	-	dB
		at −60 dBFS; A-weighted	-	−50	−45	dB
S/N	signal-to-noise ratio	code = 0; A-weighted	107	114	-	dB
α_{cs}	channel separation		-	117	-	dB

Table 66: AC characteristics *…continued*
$V_{DDD} = V_{DDA(AD)} = V_{DDA(DA)} = 3.3$ V; $f_i = 1$ kHz; $T_{amb} = 25$ °C; $R_L = 22$ kΩ; sampling frequency $f_s = 48$ kHz; all voltages referenced to ground (pins V_{SS}); unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Single-ended mode						
$V_{o(rms)}$	output voltage (RMS value)	at 0 dBFS digital input	-	1.0	-	V
ΔV_o	output voltage unbalance between channels		-	<0.1	-	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dBFS	-	−90	-	dB
		at −20 dBFS	-	−85	-	dB
		at −60 dBFS; A-weighted	-	−45	-	dB
S/N	signal-to-noise ratio	code = 0; A-weighted	-	110	-	dB
α_{cs}	channel separation		-	114	-	dB

[1] The input voltage can be up to 2 V (RMS) when the current through the ADC input pin is limited to approximately 1 mA by using a series resistor.

[2] The input voltage to the ADC scales proportionally with the power supply voltage.

16. Timing

Table 67: Timing
$V_{DDD} = V_{DDA(AD)} = V_{DDA(AD)} = 2.7$ V to 3.6 V; $T_{amb} = -20$ °C to +85 °C; typical timing specified at sampling frequency $f_s = 48$ kHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
System clock; see Figure 16						
T_{sys}	system clock cycle time	[1]				
		$f_{sys} = 256f_s$	35	81	780	ns
		$f_{sys} = 384f_s$	23	54	520	ns
		$f_{sys} = 512f_s$	17	41	390	ns
		$f_{sys} = 768f_s$	17	27	260	ns
t_{CWL}	system clock LOW time	$f_{sys} < 19.2$ MHz	$0.3T_{sys}$	-	$0.7T_{sys}$	ns
		$f_{sys} \geq 19.2$ MHz	$0.4T_{sys}$	-	$0.6T_{sys}$	ns
t_{CWH}	system clock HIGH time	$f_{sys} < 19.2$ MHz	$0.3T_{sys}$	-	$0.7T_{sys}$	ns
		$f_{sys} \geq 19.2$ MHz	$0.4T_{sys}$	-	$0.6T_{sys}$	ns
I²S-bus interface						
Serial data of audio ADC and DAC; see Figure 17						
f_{BCK}	audio bit clock frequency	[2]	-	-	12.8	MHz
$T_{cy(BCK)}$	BCK cycle time		-	-	78	ns
t_{BCKH}	bit clock HIGH time		30	-	-	ns
t_{BCKL}	bit clock LOW time		30	-	-	ns
t_r	rise time		-	-	20	ns
t_f	fall time		-	-	20	ns
$t_{su(WS)}$	word select set-up time		10	-	-	ns
$t_{h(WS)}$	word select hold time		10	-	-	ns
$t_{su(DATAI)}$	data input set-up time		10	-	-	ns

Table 67: Timing *...continued*

$V_{DDD} = V_{DDA(AD)} = V_{DDA(AD)}$ = 2.7 V to 3.6 V; T_{amb} = –20 °C to +85 °C; typical timing specified at sampling frequency f_s = 48 kHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{h(DATAI)}$	data input hold time		10	-	-	ns
$t_{h(DATAO)}$	data output hold time		0	-	-	ns
$t_{d(DATAO-BCK)}$	data output to bit clock delay		-	-	30	ns
$t_{d(DATAO-WS)}$	data output to word select delay		-	-	30	ns
Serial data of voice ADC						
f_{BCKV}	voice bit clock frequency	[2]	-	-	6.4	MHz
$T_{cy(BCKV)}$	BCKV cycle time		-	-	156	ns
t_{BCKVH}	bit clock HIGH time		50	-	-	ns
t_{BCKVL}	bit clock LOW time		50	-	-	ns
t_r	rise time		-	-	20	ns
t_f	fall time		-	-	20	ns
$t_{su(WSV)}$	word select set-up time		10	-	-	ns
$t_{h(WSV)}$	word select hold time		10	-	-	ns
$t_{h(DATAV)}$	data output hold time		0	-	-	ns
$t_{d(DATAV-BCKV)}$	data output to bit clock delay		-	-	30	ns
$t_{d(DATAV-WSV)}$	data output to word select delay		-	-	30	ns
$t_{d(WSV-BCKV)}$	word select to bit clock delay	WSV-out mode	–30	-	+30	ns
L3-bus interface; see Figure 18 and 19						
L3CLOCK timing						
$f_{cy(CLK)L3}$	L3CLK frequency		-	-	2000	kHz
$T_{cy(CLK)L3}$	L3CLOCK cycle time		500	-	-	ns
$t_{CLK(L3)H}$	L3CLOCK HIGH time		250	-	-	ns
$t_{CLK(L3)L}$	L3CLOCK LOW time		250	-	-	ns
L3MODE timing						
$t_{su(L3)A}$	L3MODE set-up time in address mode		190	-	-	ns
$t_{h(L3)A}$	L3MODE hold time in address mode		190	-	-	ns
$t_{su(L3)D}$	L3MODE set-up time in data transfer mode		190	-	-	ns
$t_{h(L3)D}$	L3MODE hold time in data transfer mode		190	-	-	ns
$t_{stp(L3)}$	L3MODE stop time in data transfer mode		190	-	-	ns
L3DATA timing						
$t_{su(L3)DA}$	L3DATA set-up time in data transfer and address mode		190	-	-	ns
$t_{h(L3)DA}$	L3DATA hold time in data transfer and address mode		30	-	-	ns
$t_{d(L3)R}$	L3DATA delay time for read data		0	-	50	ns
$t_{dis(L3)R}$	L3DATA disable time for read data		0	-	50	ns

Table 67: Timing *…continued*

$V_{DDD} = V_{DDA(AD)} = V_{DDA(AD)}$ = 2.7 V to 3.6 V; T_{amb} = –20 °C to +85 °C; typical timing specified at sampling frequency f_s = 48 kHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I^2C-bus interface timing; see Figure 20						
SCL timing						
f_{SCL}	SCL clock frequency		0	-	400	kHz
t_{LOW}	SCL LOW time		1.3	-	-	µs
t_{HIGH}	SCL HIGH time		0.6	-	-	µs
t_r	rise time SDA and SCL	[3]	20 + 0.1C_b	-	300	ns
t_f	fall time SDA and SCL	[3]	20 + 0.1C_b	-	300	ns
SDA timing						
t_{BUF}	bus free time between STOP and START condition		1.3	-	-	µs
$t_{SU;STA}$	set-up time repeated START		0.6	-	-	µs
$t_{HD;STA}$	hold time START condition		0.6	-	-	µs
$t_{SU;DAT}$	data set-up time		100	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	µs
$t_{SU;STO}$	set-up time STOP condition		0.6	-	-	µs
t_{SP}	pulse width of spikes	[4]	0	-	50	ns
C_b	capacitive load for each bus line		-	-	400	pF

[1] The system clock should not exceed 58 MHz in any mode.

[2] The bit clock frequency should not exceed 256 times the corresponding sampling frequency.

[3] C_b is the total capacitance for each bus line.

[4] To be suppressed by the input filter.

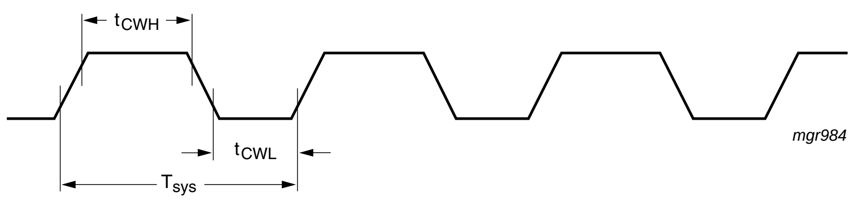


Fig 16. System clock timing

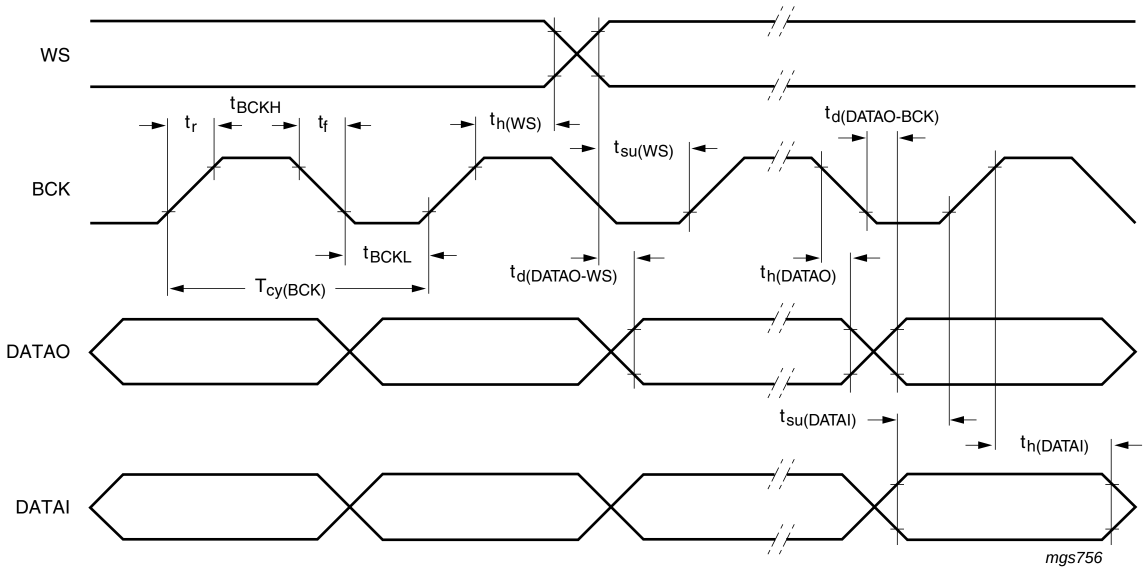


Fig 17. I²S-bus serial interface timing

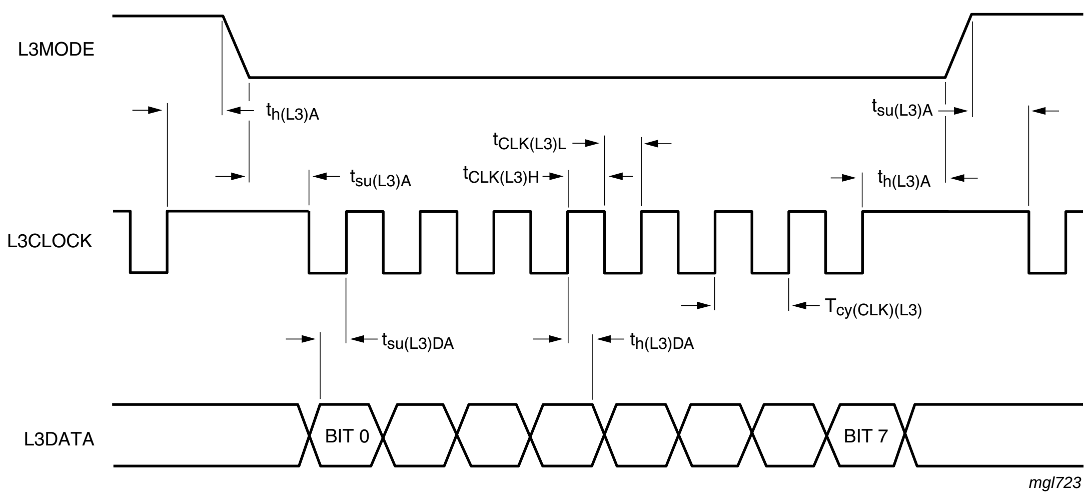


Fig 18. L3-bus address mode timing

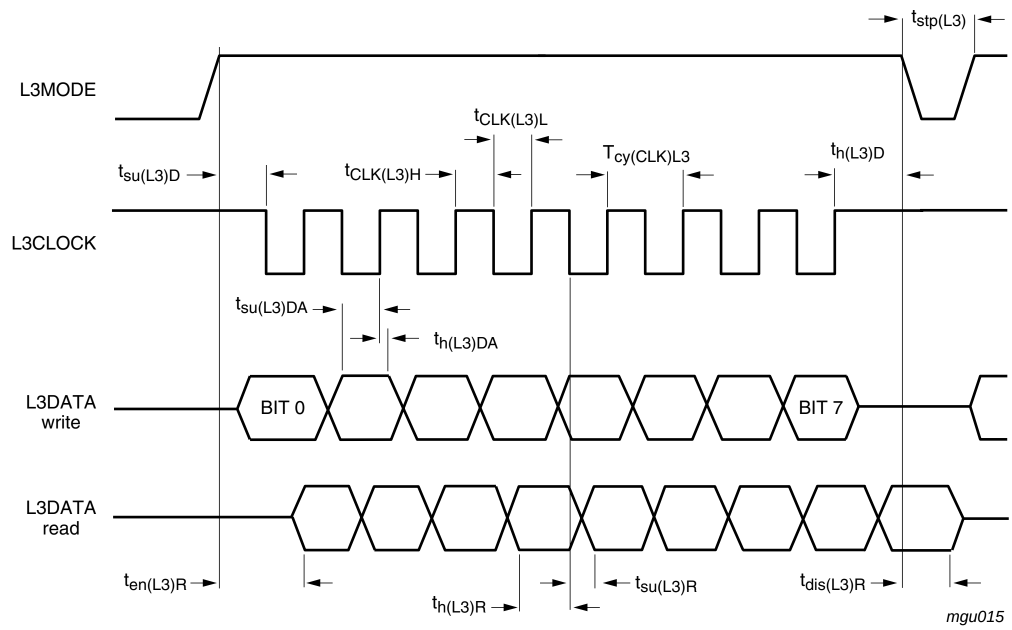


Fig 19. L3-bus data transfer (write and read) mode timing

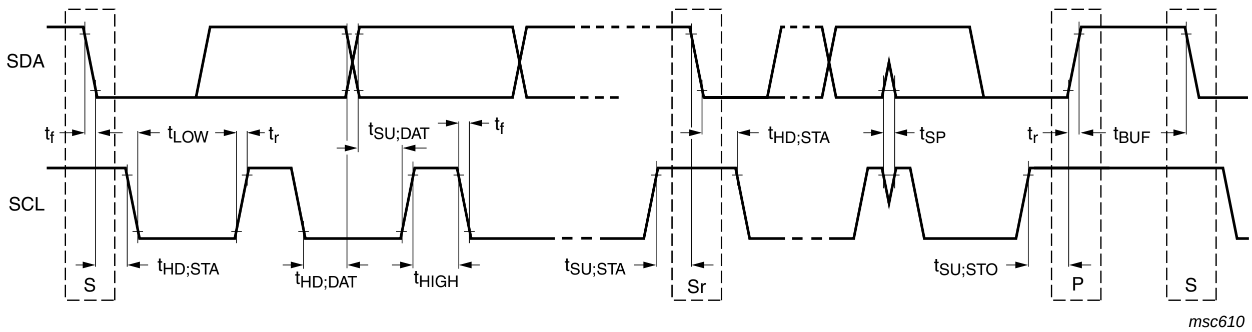
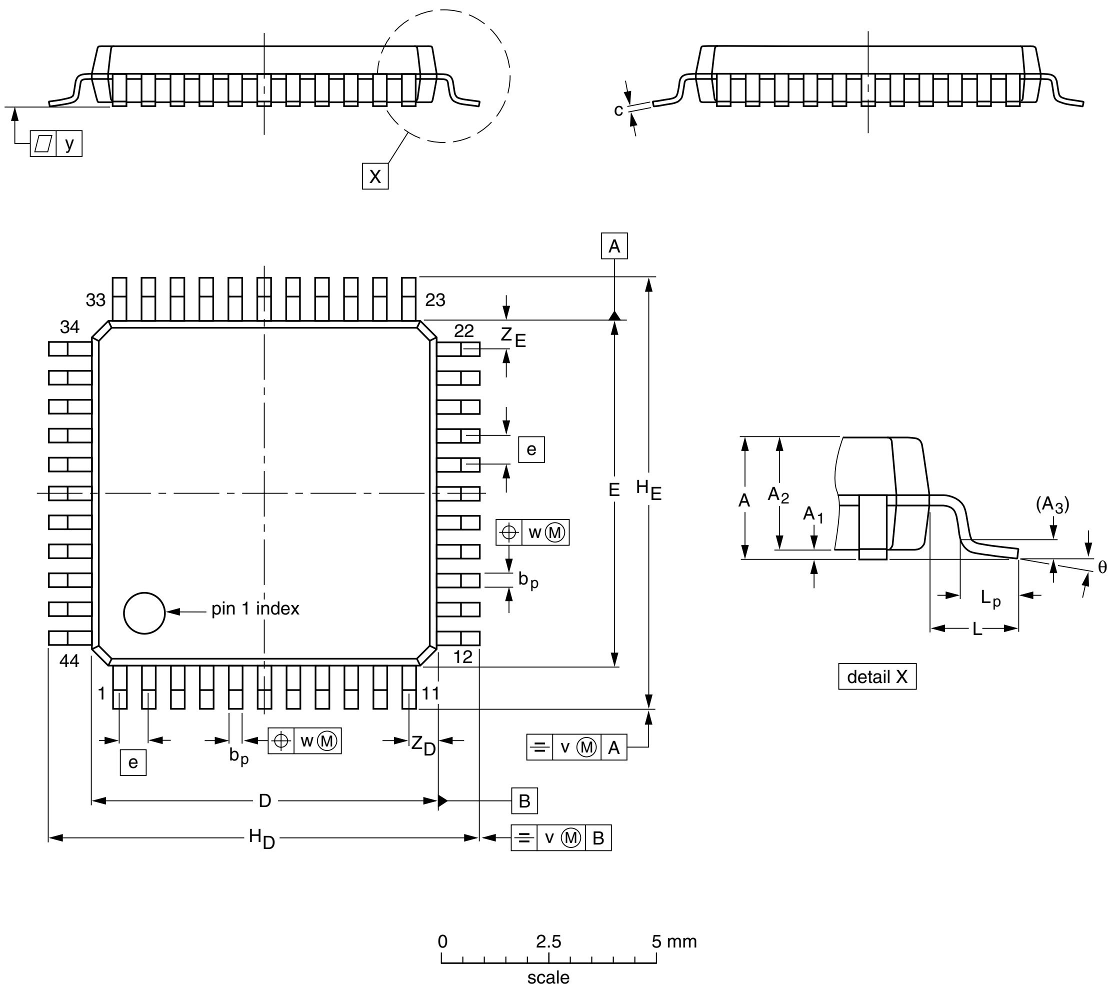


Fig 20. I²C-bus timing

17. Package outline

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	2.1	0.25 0.05	1.85 1.65	0.25	0.4 0.2	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT307-2						~~97-08-01~~ 03-02-25

Fig 21. Package outline SOT307-2 (QFP44)

18. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

19. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

19.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

19.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

19.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

19.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 22) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 68 and 69

Table 68. SnPb eutectic process (from J-STD-020C)

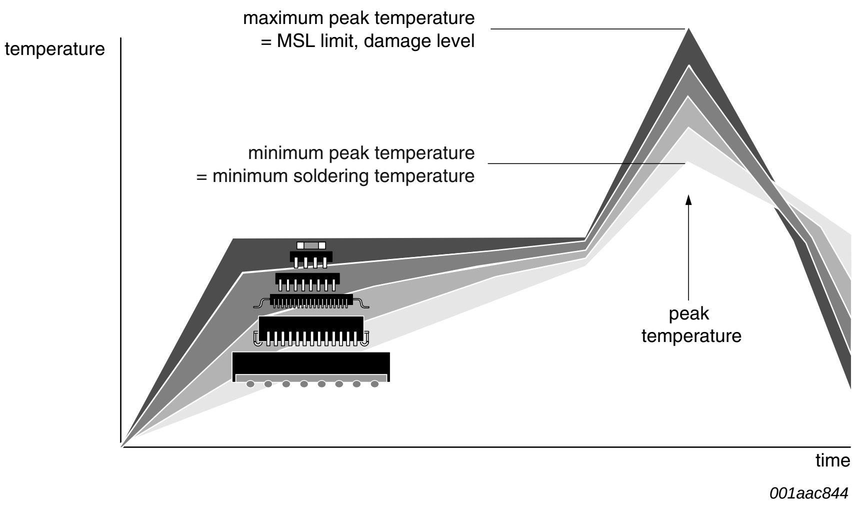
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 69. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 22.



MSL: Moisture Sensitivity Level

Fig 22. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

20. Revision history

Table 70: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
UDA1338H v.4	20100518	Product data sheet	-	-	UDA1338H_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section “Test information” and subsection “Quality information” removed. • Section 18 “Handling information”: text updated • Section 19 “Soldering of SMD packages”: title changed, text updated				
UDA1338H_3	20050216	Product data sheet	-	9397 750 14389	UDA1338H_2
UDA1338H_2	021121	Preliminary specification	-	9397 750 10089	UDA1338H_1
UDA1338H_1	020523	Preliminary specification	-	9397 750 09319	-

21. Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

21.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

21.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

21.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

22. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

23. Contents

1 General description . . . 1
2 Features and benefits . . . 1
2.1 General . . . 1
2.2 Multiple format data interface . . . 2
2.3 Digital sound processing . . . 2
2.4 Advanced audio configuration . . . 2
3 Applications . . . 2
4 Quick reference data . . . 2
5 Ordering information . . . 3
6 Block diagram . . . 4
7 Pinning information . . . 5
7.1 Pinning . . . 5
7.2 Pin description . . . 5
8 Functional description . . . 7
8.1 System clock . . . 7
8.2 Audio analog-to-digital converter (audio ADC) . 8
8.3 Voice analog-to-digital converter (voice ADC) . 8
8.4 Decimation filter of audio ADC . . . 8
8.5 Decimation filter of voice ADC . . . 9
8.6 Interpolation filter of DAC . . . 9
8.7 Noise shaper of DAC . . . 9
8.8 Digital mixer . . . 9
8.9 Audio digital-to-analog converters . . . 10
8.10 Power-on reset . . . 10
8.11 Audio digital interface . . . 11
8.12 Voice digital interface . . . 14
8.13 DSD mode . . . 14
8.14 Microcontroller interface mode . . . 15
9 L3-bus interface . . . 15
9.1 General . . . 15
9.2 Device addressing . . . 16
9.3 Register addressing . . . 16
9.4 Data write mode . . . 18
9.5 Data read mode . . . 18
10 I²C-bus interface . . . 19
10.1 General . . . 19
10.2 Characteristics of the I²C-bus . . . 19
10.3 Bit transfer . . . 19
10.4 Byte transfer . . . 20
10.5 Data transfer . . . 20
10.6 Start and stop conditions . . . 20
10.7 Acknowledgment . . . 20
10.8 Device address . . . 21
10.9 Register address . . . 21
10.10 Write and read data . . . 22
10.11 Write cycle . . . 22
10.12 Read cycle . . . 22
11 Register mapping . . . 23
11.1 Address mapping . . . 23
11.2 Register mapping . . . 25
11.3 System settings . . . 27
11.4 Audio ADC and DAC subsystem settings . . . 28
11.5 Voice ADC system settings . . . 30
11.6 Status output register (read only) . . . 31
11.7 DAC channel selection . . . 32
11.8 DAC features settings . . . 33
11.9 DAC channel 1 to channel 6 settings . . . 35
11.10 DAC mixing channel settings . . . 35
11.11 Audio ADC 1 and ADC 2 input amplifier gain settings . . . 36
11.12 Voice ADC gain settings . . . 37
11.13 Supplemental settings 1 . . . 37
11.14 Supplemental settings 2 . . . 38
12 Limiting values . . . 39
13 Thermal characteristics . . . 39
14 Static characteristics . . . 40
15 Dynamic characteristics . . . 41
16 Timing . . . 43
17 Package outline . . . 48
18 Handling information . . . 49
19 Soldering of SMD packages . . . 49
19.1 Introduction to soldering . . . 49
19.2 Wave and reflow soldering . . . 49
19.3 Wave soldering . . . 49
19.4 Reflow soldering . . . 50
20 Revision history . . . 52
21 Legal information . . . 53
21.1 Data sheet status . . . 53
21.2 Definitions . . . 53
21.3 Disclaimers . . . 53
21.4 Trademarks . . . 54
22 Contact information . . . 54
23 Contents . . . 55

Date of release: 18 May 2010
Document identifier: UDA1338H