PERICOM Enabling Serial Connectivity

Product Brief

Product: **SlimLine™ PCI Express® to PCI Bridge**

Part Numbers: **PI7C9X112SL**

Product Description

The PI7C9X112SL is the latest addition to Pericom's PCI Express® Bridge SlimLine™ family of solutions. With the PI7C9X112SL, users can expect a x1 PCI Express to 32bit/66MHz PCI bridge with high performance, very low power consumption, and a small footprint. PI7C9X112SL offers the most effective forward bridging solution to platforms with high bandwidth requirement. The typical usage for this device is high volume applications requiring a "bridge" from legacy PCI products to new PCI Express based systems, or applications requiring a "bridge" to support multiple legacy PCI systems. The PI7C9X112SL is a versatile device that can be deployed in applications including desktops, graphics cards, combo cards, PC peripherals, MFP Printer and video surveillance systems.

Industry Specifications Compliance

- *PCI Express Base Specification*, Rev. 1.1
- *PCI Express CEM Specification*, Rev. 1.0a
- *PCI Express to PCI/PCI-X Bridge Specification*, Rev. 1.0
- *PCI-to-PCI Bridge Architecture Specification*, Rev. 1.2
- *PCI Local Bus Specification*, Rev. 3.0
- *PCI Hot-Plug Specification*, Rev. 1.1
- *PCI SHPC and Subsystem Specification*, Rev. 1.0
- *PCI Mobile Design Guide*, Version 1.1
- System Management (SM) Bus, Version 2.0
- *PCI Bus PM Interface Specification*, Rev. 1.1
- *Advanced Configuration and Power Interface Specification*, Rev. 2.0

General Feature Set

- Fully PCIe 1.1 Compliant
  - Forward – PCI Express primary, PCI secondary
- Maximum Payload Size – Up to 512 bytes
- Ultra Low Power Modes
  - Critical for mobile applications
- Support for up to 8 PCI Bus Masters with external 4 to 8 demux logic
- Industrial Temp Compliant (-40C~+85C)
- Two level internal arbitration
- Typical Power: <460mW
- GPIO Support - 4 dedicated bi-directional
- When external arbiter is used:
  - 4 additional outputs
  - 4 additional inputs
- Masquerade support
  - User defined vendor, device, revision, subsystem device, and subsystem vendor ID
- Large 10KB Buffer
  - 4KB for upstream reads, 2KB for downstream reads & 2KB for writes per port
- Access to Extended Configuration Registers From PCI side in Reverse Mode
- Tiny 14 x 14mm, 128-pin QFP Package

PCI Express Features

- Virtual Isochronous Support
  - Upstream TC 1 – 7 generation
  - Downstream TC 1 – 7 mapping
- 16-bit CRC, LCRC (32-bit)
- ECRC and Advanced Error Reporting
- Error Forwarding (Data Poisoning)
- Lane Reversal (Polarity Toggle)
- VDDAUX Support (1.0V)

PCI Features

- 3.3V Signaling with 5V I/O Tolerance
- PME# Support
- 16-bit Address Decode for VGA
- VAUX Support (3.3V)
- Subsystem Device and Subsystem Vendor ID
- MSI and INT Support
- SM Bus
  - PHY, data link, network layer, PEC, ARP, etc.
- I2C Serial EEPROM Support

Application Example