ML631 Virtex-6 HXT FPGA Packet Processor/Traffic Manager Evaluation Board

User Guide

UG841 (v1.0) March 9, 2012

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/09/2012	1.0	Initial Xilinx release.

Table of Contents

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Chapter 1

ML631 Board Features and Components

This user guide describes the components and features of the ML631 Virtex-6 HXT FPGA Packet Processor/Traffic Manager (PP/TM) evaluation board. The ML631 board provides the hardware environment for characterizing and evaluating the GTX and GTH transceivers available on the Virtex-6 XC6VHXT565-2FFG1923C FPGA.

ML631 Board Features

Details for the following features are described in Feature Descriptions, page 6.

- Two Virtex-6 XC6VHXT565-2FFG1923C FPGAs
- Onboard power regulators for all necessary voltages with power status LEDs
- Two types of external power supply jacks (12V brick DIN4 type, PC ATX type)
- USB JTAG configuration port for use with USB A to Mini-B cable
- System ACE™ controller with companion SanDisk® CompactFlash® socket
- General purpose pushbuttons, DIP switches, and LEDs for each FPGA
- VGA 2 x 5 male debug header for the U2 FPGA
- USB-to-UART bridge with USB Mini-B connector for the U2 FPGA
- I^2C bus hosting EEPROM and clock sources
- A separate SiTime fixed 200-MHz 2.5V LVDS oscillator wired to the global clock inputs of each FPGA
- Six pairs of differential clock input SMA connectors
- Six I^2C programmable Silicon Labs Si570 3.3V LVDS 10-MHz to 810-MHz oscillators
- Two differential input 8 x 8 crosspoint switches providing 16 selectable differential clock sources
- Three sets of plug and receptacle FCI Airmax 120-pin connectors, two implementing the Interlaken interconnect protocol and one available for an OTN/OTN client interface
- 9 x 32-bit DDR3 memory on the U1 FPGA
- 4 x 16-bit DDR3, 2 x 18-bit DDR2, and 2 x 36-bit QDRII+ memories on the U2 FPGA
- NetLogic Microsystems NL92000 series network processor [ternary content addressable memory (TCAM)] adjunct on the U2 FPGA

The ML631 board block diagram is shown in Figure 1-1.

Caution! The ML631 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

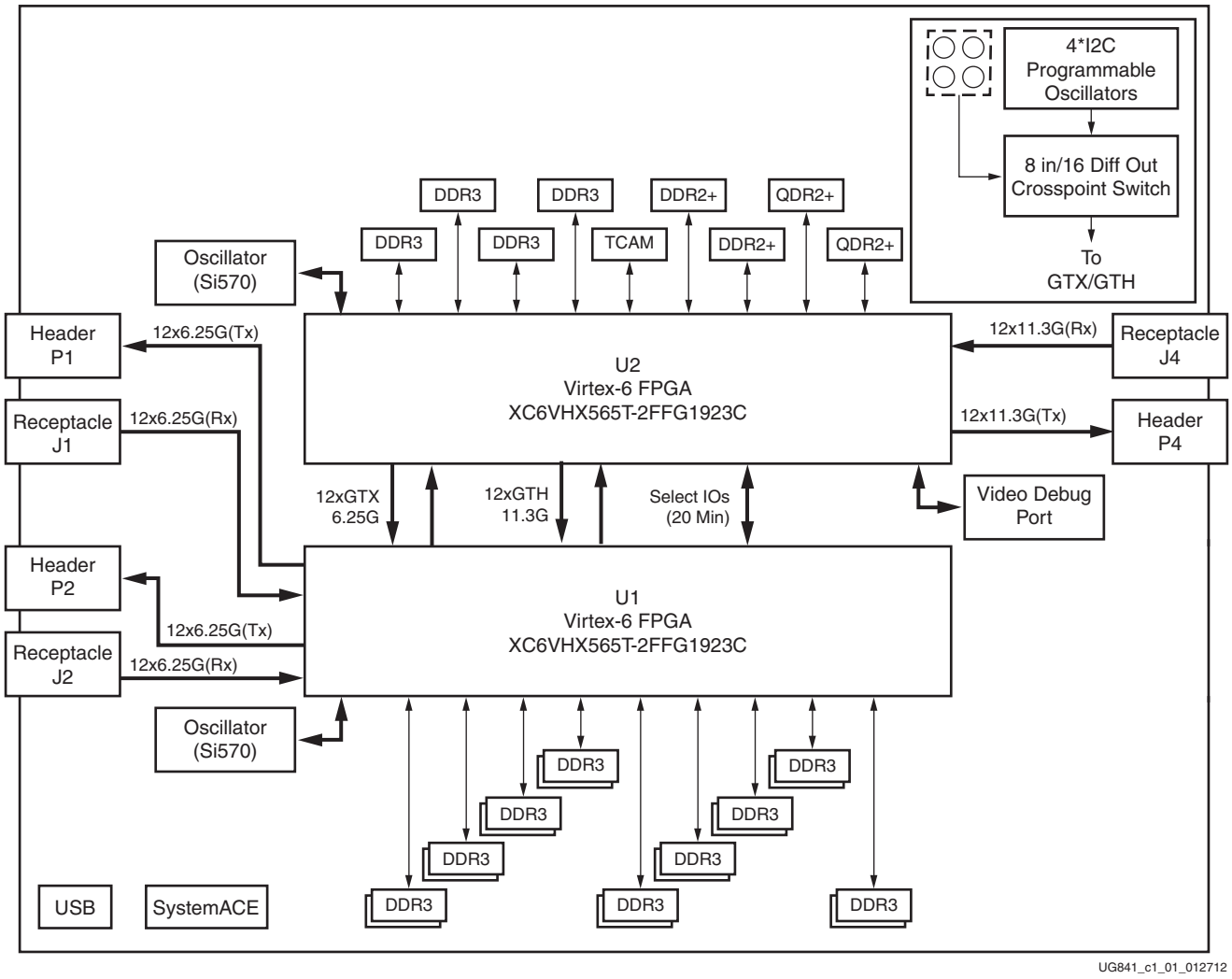

Figure 1-1: **ML631 Board Block Diagram**

Feature Descriptions

This section is intended to be used with the *ML631 Schematic* [Ref 1]. The ML631 board hosts a complicated clocking system and intricate FPGA-to-FPGA and Interlaken connector connectivity that the schematic helps clarify. Refer to the schematic pages associated with the circuitry described in each section of this detailed description [Ref 1].

Figure 1-2 shows the ML631 board. Each numbered feature that is referenced in Figure 1-2 is described in Table 1-1 and the other sections in this chapter.

Note: The image in Figure 1-2 is for reference only. It might not reflect the current revision of the board.

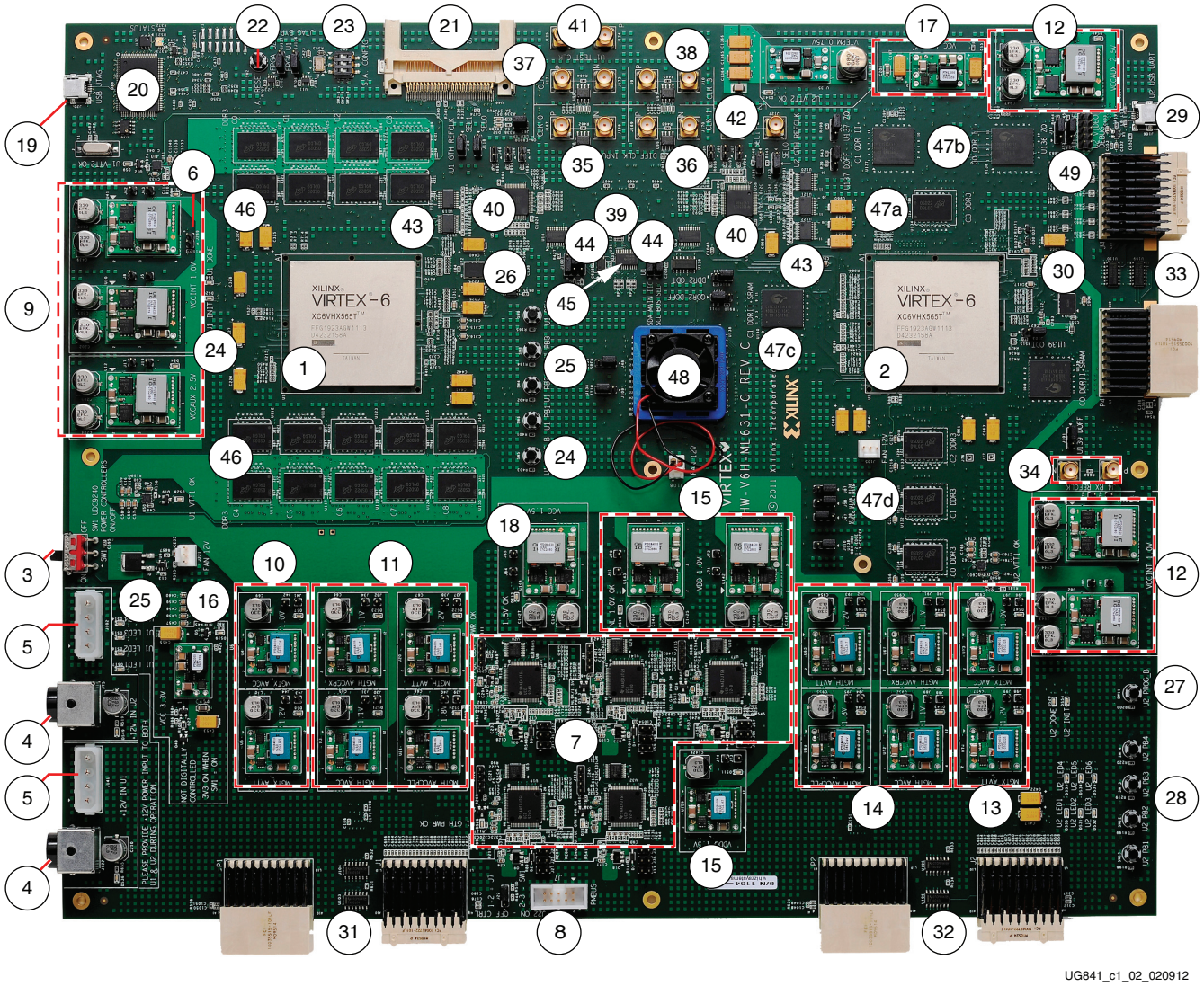

Figure 1-2: **ML631 Board Components**

Table 1-1 summarizes features referenced in Figure 1-2, and lists the page in the *ML631 Schematic* that contains more details [Ref 1].

Table 1-1: **ML631 Board (Revision C) Features and Corresponding Schematic References**

Number	Feature	Notes	Schematic Page
1	Virtex-6 HXT FPGA	U1 XC6VHXT565-2FFG1923C	2
2	Virtex-6 HXT FPGA	U2 XC6VHXT565-2FFG1923C	3
3	On-Off soft slide switch	SW1	65
4	DIN-4 12V input connectors	J122 for the U1 FPGA, J75 for the U2 FPGA	63, 127
5	ATX 4-pin 12V input connectors	J141 for the U1 FPGA, J102 for the U2 FPGA	63, 127
6	Voltage regulator inhibit header	J289 (used only for CM power config.)	66

Table 1-1: **ML631 Board (Revision C) Features and Corresponding Schematic References *(Cont'd)***

Number	Feature	Notes	Schematic Page
7	TI power system controllers	U8, U19, U32, U77, U141	65, 70, 75, 129, 134
8	PMBus connector	J7 for TI Fusion GUI GPIO adapter pod	65
9	U1 V_{CCINT}, V_{CCAUX} TI regulators	U10/U41 V_{CCINT}, U12 V_{CCAUX} (3 x TI PTD08A020W)	66, 67
10	U1 GTX TI regulators	U4 AVCC, U5 AVTT (2 x TI PTD08A010W)	76, 77
11	U1 GTH TI regulators	U3 AVCC, U14 AVCCRX, U20 AVTT, U21 AVCCPLL (1 x PTD08A010W, 3 x PTD08A006W)	71, 72, 73, 74
12	U2 V_{CCINT}, V_{CCAUX} TI regulators	U81/U82 V_{CCINT}, U83 V_{CCAUX} (3 x TI PTD08A020W)	68, 69
13	U2 GTX TI regulators	U73 AVCC, U74 AVTT (2 x TI PTD08A010W)	78, 79
14	U2 GTH TI regulators	U72 AVCC, U67 AVCCRX, U68 AVTT, U69 AVCCPLL (1 x PTD08A010W, 3 x PTD08A006W)	130, 131, 132, 133
15	NetLogic Microsystems processor TI regulators	U142/U143 V_{DD}, U129 V_{DDQ} (2 x TI PTD08A020W, 1 x PTD08A006W)	135, 136
16	ML631 board-wide 3.3V regulator	U6 VCC3V3 TI PTH12000W	8
17	ML631 board-wide 1.8V regulator	U7 VCC1V8 TI PTH12000W	83
18	ML631 board-wide 1.5V regulator	U144 VCC1V5 PTD08A020W	137
19	USB JTAG mini-USB connector	J20	6
20	Embedded JTAG circuits	U48 CY7C68013A, U45 XC2C256	6
21	System ACE controller, CompactFlash socket	U47 XACCE-TQ144I (bottom of board), U46 CF socket	5
22	System ACE controller reset pushbutton switch	SW2	5
23	CompactFlash image select switch	SW3	5
24	U1 PROG PB, INIT, and DONE LEDs	SW5 PROG pushbutton, DS20 INIT, DS6 DONE	16
25	U1 user LEDs and pushbuttons	DS17, 16, 15, 14 user LED1, 2, 3, 4, SW6, 4, 8, 9 user PB1, 2, 3, 4	16
26	U1 fixed 200-MHz system clock	U22 SI9102 2.5V 20 PPM 200.0000 MHz LVDS	16
27	U2 PROG PB, INIT, and DONE LEDs	SW11 PROG pushbutton, DS54 INIT, DS29 DONE	82
28	U2 user LEDs and pushbuttons	DS30–DS35 are user LED1-user LED6; SW15,12,13, and 14 are user PB1–4	82
29	U2 USB UART mini-USB connector	J106	81
30	U2 fixed 200-MHz system clock	U63 SI9102 2.5V 20 PPM 200.0000 MHz LVDS	82

Table 1-1: **ML631 Board (Revision C) Features and Corresponding Schematic References *(Cont'd)***

Number	Feature	Notes	Schematic Page
31	U1 FCI Airmax connector pair	P1, J1 (connected to GTX transceivers)	26, 27
32	U1 FCI Airmax connector pair	P2, J2 (connected to GTX transceivers)	23, 24
33	U2 FCI Airmax connector pair	P4, J4 (connected to GTH transceivers)	87, 88
34	U2 J4 RX REFCLK input SMA connectors	SMA J134, J135	88
35	SMA input clock differential pair	SMA J167, J168, U98 ICS85311 1-to-2 LVPECL clock buffer	9
36	SMA input clock differential pair	SMA J169, J170, U99 ICS85311 1-to-2 LVPECL clock buffer	9
37	SMA input clock differential pair	SMA J171, J172, U96 ICS85311 1-to-2 LVPECL clock buffer	9
38	SMA input clock differential pair	SMA J9, J10, U97 ICS85311 1-to-2 LVPECL clock buffer	9
39	ML631 programmable clock sources	U43, U44, U51, U52 Si570 each with U53, U54, U55, U56 ICS85311 1-to-2 LVPECL clock buffers (bottom of board)	10
40	ML631 8 x 8 crosspoint clock switches	U57, U58 TI SN65LVP408PAP	14
41	U1 differential test clock input SMA	SMA J124, J125, U126 ICS854S006 1-to-6 LVDS clock buffer	12
42	U2 differential test clock input SMA	SMA J126, J127, U127 ICS854S006 1-to-6 LVDS clock buffer	13
43	ML631 differential clock multiplexer circuits	5 each ICS85356 U102, U115, U120, U121, U122	12, 13
44	U1, U2 programmable clock sources	U64 Si570 (bottom of board) U13 ICS854S006 1-to-6 LVDS clock buffer; U65 Si570 (bottom of board) U18 ICS854S006 1-to-6 LVDS clock buffer	15, 81
45	ML631 I^2C bus residents	U59 M24C02 EEPROM, U31 PCA9548 bus-expander	10
46	U1 memory system	9x 32-bit DDR3 chip pairs of MT41J128M16HA, controller C0: U24, U76; C1: U25, U78; C2: U84, U88; C3: U89, U101; C4: U111, U112; C5: U117, U118; C6: U119, U123; C7: U124, U125; C8: U130, U131	29–55
47	U2 memory system	See 47a, 47b, 47c	
47a	DDR3	4x 16-bit DDR3 MT41J128M16HA, controller C0: U70; C1: U132; C2: U133; C3: U134	92–99
47b	DDR2 SRAM	2x 18-bit DDR2 CY7C12481KV18, controller C0: U139; C1: U140	100–103
47c	QDRII+	2x 36-bit QDR2+ CY7C1565KV18, controller C0: U136; C1: U137	104–113

Table 1-1: **ML631 Board (Revision C) Features and Corresponding Schematic References *(Cont'd)***

Number	Feature	Notes	Schematic Page
48	NetLogic Microsystems processor	U138 NL9256EFVH-400H	117–118
49	U2 VGA debug connector	J60 2x5 male pin header	119

Default Shunts

A list of shunts and their required positions for board operation is provided in Appendix A, Default Shunt Positions.

Monitoring Voltage and Current

Voltage and current monitoring and control are available for all power rails except the fixed 3.3V and 1.8V using the Texas Instruments' Fusion Digital Power graphical user interface (GUI). All onboard TI power controllers are wired to the same PMBus. The PMBus connector, J7, is provided for use with the TI GPIO interface adapter (PMBus pod) and associated TI Fusion Digital Power GUI.

More information about the power system components used by the ML631 board is available from the Texas Instruments digital power website [Ref 18].

U1 and U2 FPGAs

See Figure 1-2 callouts [1, 2].

The ML631 board hosts two Virtex-6 XC6VHXT565-2FFG1923C FPGAs. Each FPGA provides six four-transceiver GTH Quads and ten four-transceiver GTX Quad high-speed interfaces.

Appendix D, Additional Resources provides references to ML631 board documents, files, and resources.

Board Power

See Figure 1-2 callouts [3, 4, 5].

The ML631 board is powered through two 4-pin DIN right angle connectors, J122 and J75, using the two 12V, 15A AC adapters included with the board.

Power can also be provided through J141 and J102 ATX hard disk 4-pin power connectors. J122 (4-pin DIN connector) and J141 (ATX connector) are wired in parallel, as are J75 and J102. When the board power is supplied through J122 and J75, 12 VDC is present at the ATX connectors J141 and J102 and vice versa.

Note: Use of a switchable multiple outlet AC power strip is recommended for providing mains power to the two AC adapters. Both adapters can be turned on and off simultaneously via the power strip on/off switch.

> ***Caution!*** Only use two power supplies of the same type. Power the ML631 board through two connectors at the same time (J122 and J75 or J141 and J102, depending on power supply type). Do NOT apply power to all four power input connectors J122/J75 and J141/J102 at the same time. Doing so can damage the ML631 board and void the board warranty.

When the AC adapters are connected to the ML631 board and turned on through the AC power strip, 12 VDC is applied to the 12V power planes. Green LED indicators DS36 and DS49 (adjacent to each 4-pin DIN connector) illuminate to indicate 12V power is on.

Switch SW1

The ML631 board U1 and U2 FPGA power regulators are turned on and off by slide switch SW1. When this switch is in the ON position, power is applied to the FPGAs, and the green LEDs adjacent to each active regulator illuminate.

Figure 1-3 shows the power system block diagram for the U1 FPGA and part of the U2 FPGA. Circuit details are available in the *ML631 Schematic* pages 8, 63–80, 83 and 127–138 as noted in the various function blocks [Ref 1].

Power System

Figure 1-3 shows the onboard power supply architecture for the U1 FPGA.

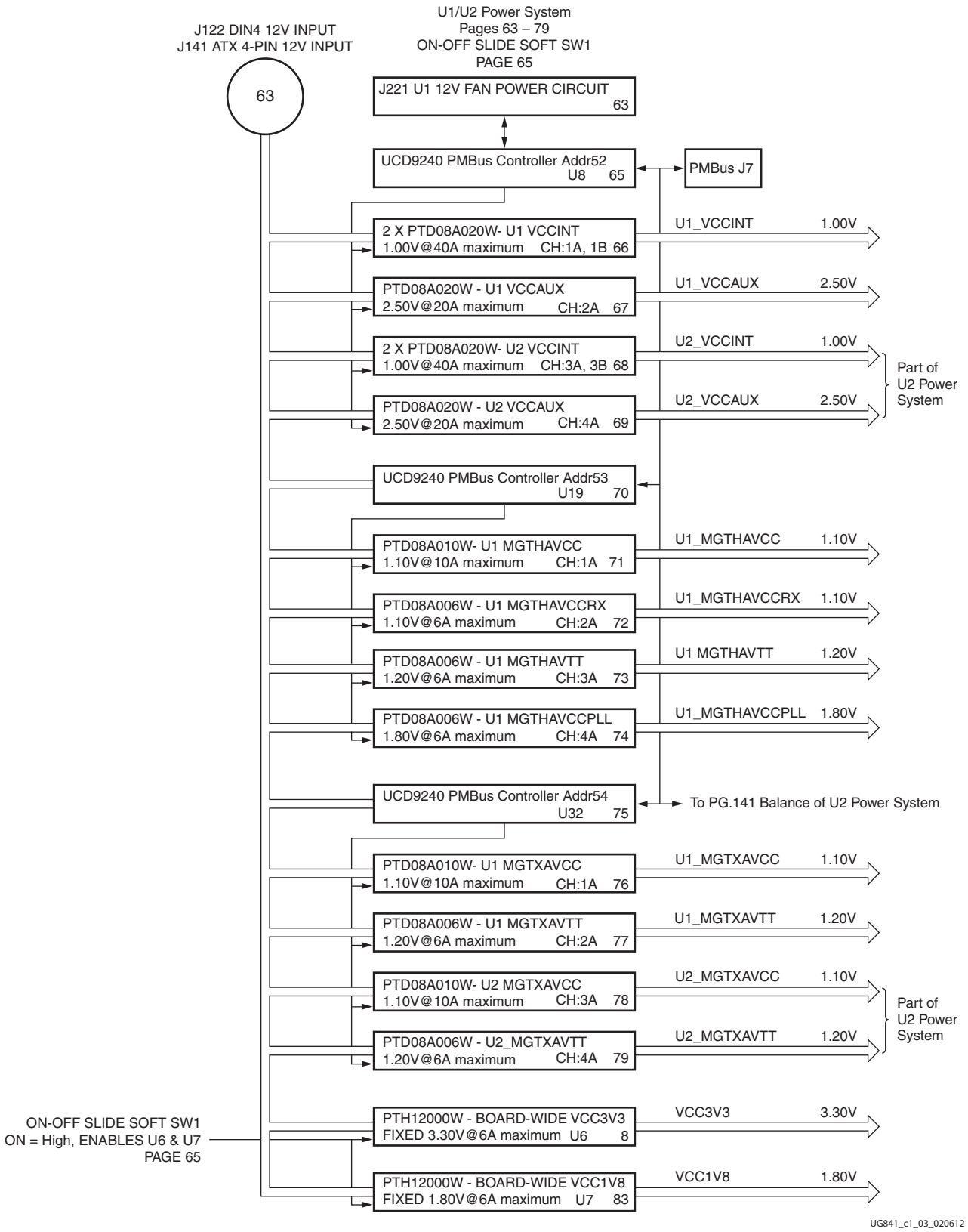

Figure 1-3: **Power Block Diagram for the U1 FPGA**

Figure 1-4 shows the onboard power supply architecture for the U2 FPGA. Circuit details are available in *ML631 Schematic* pages 127 through 137 as noted in the various function blocks [Ref 1].

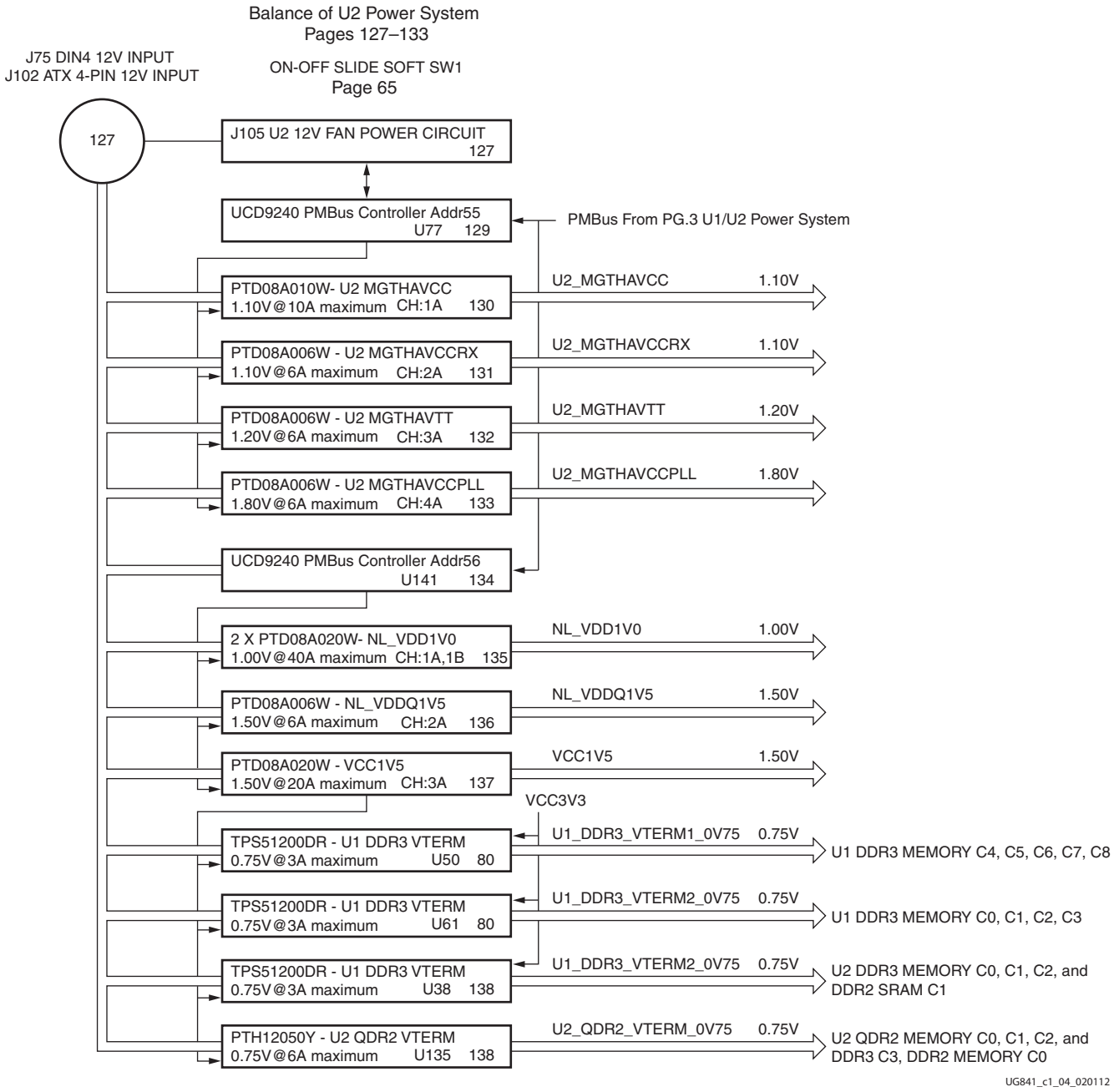

Figure 1-4: **Power Block Diagram for the U2 FPGA**

The ML631 board uses power regulators and PMBus-compliant digital PWM system controllers from Texas Instruments to supply the U1 and U2 voltages listed in Table 1-2.

Table 1-2: **Onboard Power System Devices**

Device	Ref. Des.	Description	Power Rail Net Name	Typical Voltage
U1 and U2 Core Voltage Controller and Regulators				
UCD9240PFC	U8	PMBus-compliant digital PWM system controller (address = 52)		
PTD08A020W	U10	Adjustable switching regulator 20A, 0.6V to 3.6V, 1 of 2 phases	U1_VCCINT	1.0V
PTD08A020W	U41	Adjustable switching regulator 20A, 0.6V to 3.6V, 2 of 2 phases	U1_VCCINT	1.0V
PTD08A020W	U12	Adjustable switching regulator 20A, 0.6V to 3.6V	U1_VCCAUX	2.5V
PTD08A020W	U81	Adjustable switching regulator 20A, 0.6V to 3.6V, 1 of 2 phases	U2_VCCINT	1.0V
PTD08A020W	U82	Adjustable switching regulator 20A, 0.6V to 3.6V, 2 of 2 phases	U2_VCCINT	1.0V
PTD08A020W	U83	Adjustable switching regulator 20A, 0.6V to 3.6V	U2_VCCAUX	2.5V
U1 GTH Transceiver Voltage Controller and Regulators				
UCD9240PFC	U19	PMBus-compliant digital PWM system controller (address = 53)		
PTD08A010W	U3	Adjustable switching regulator 10A, 0.6V to 3.6V	U1_MGTHAVCC	1.1V
PTD08A006W	U14	Adjustable switching regulator 10A, 0.6V to 3.6V	U1_MGTXAVCCRX	1.1V
PTD08A006W	U20	Adjustable switching regulator 10A, 0.6V to 3.6V	U1_MGTHAVTT	1.2V
PTD08A006W	U21	Adjustable switching regulator 10A, 0.6V to 3.6V	U1_MGTXAVCCPLL	1.8V
U1 and U2 GTX Transceiver Voltage Controller and Regulators				
UCD9240PFC	U32	PMBus-compliant digital PWM system controller (address = 54)		
PTD08A010W	U4	Adjustable switching regulator 10A, 0.6V to 3.6V	U1_MGTXAVCC	1.1V
PTD08A010W	U5	Adjustable switching regulator 10A, 0.6V to 3.6V	U1_MGTXAVTT	1.2V
PTD08A010W	U73	Adjustable switching regulator 10A, 0.6V to 3.6V	U2_MGTXAVCC	1.1V
PTD08A010W	U74	Adjustable switching regulator 10A, 0.6V to 3.6V	U2_MGTXAVTT	1.2V
U2 GTH Transceiver Voltage Controller and Regulators				
UCD9240PFC	U77	PMBus-compliant digital PWM system controller (address = 55)		
PTD08A010W	U72	Adjustable switching regulator 10A, 0.6V to 3.6V	U2_MGTHAVCC	1.1V
PTD08A006W	U67	Adjustable switching regulator 10A, 0.6V to 3.6V	U2_MGTXAVCCRX	1.1V
PTD08A006W	U68	Adjustable switching regulator 10A, 0.6V to 3.6V	U2_MGTHAVTT	1.2V
PTD08A006W	U69	Adjustable switching regulator 10A, 0.6V to 3.6V	U2_MGTXAVCCPLL	1.8V
U138 NetLogic and Board-Wide Voltage Controller and Regulators				
UCD9240PFC	U141	PMBus-compliant digital PWM system controller (address = 56)		

Table 1-2: **Onboard Power System Devices *(Cont'd)***

Device	Ref. Des.	Description	Power Rail Net Name	Typical Voltage
PTD08A020W	U142	Adjustable switching regulator 20A, 0.6V to 3.6V, 1 of 2 phases	NL_VDD1V0	1.0V
PTD08A020W	U143	Adjustable switching regulator 20A, 0.6V to 3.6V, 2 of 2 phases	NL_VDD1V0	1.0V
PTD08A006W	U129	Adjustable switching regulator 6A, 0.6V to 3.6V	NL_VDDQ1V5	1.5V
PTD08A020W	U144	Adjustable switching regulator 20A, 0.6V to 3.6V, 1 of 2 phases	VCC1V5	1.5V
Auxiliary Power Fixed Output Voltage Regulators				
PTH12000W	U6	Adjustable switching regulator 6A, 1.2V to 5.5V	VCC3V3	3.3V
PTH12000W	U7	Adjustable switching regulator 6A, 1.2V to 5.5V	VCC1V8	1.8V

Disabling FPGA Onboard Power

See Figure 1-2 callout [6].

All ML631 voltage regulators are disabled by installing a shunt across pins 1-2 of header J289. If 12V is supplied to the board with the J289 shunt installed, the TI power system controllers power up, and if the SW1 on-off slide switch is then switched to the ON position, all board voltage regulators remain inhibited. J289 is typically installed only for assembly house power system programming, and is not installed for standard board operation.

FPGA Configuration

See Figure 1-2 callout [19–23].

The FPGA is configured in JTAG mode only, using one of these options:

- Embedded USB JTAG circuit using USB cable (type A to Mini-B)
- System ACE controller (using a CompactFlash card loaded with bit files)

The FPGA Embedded JTAG option is enabled by connecting the Mini-B connector end of the USB cable to J20 on the ML631 board. The type A connector end of the USB cable plugs into a PC hosting a Xilinx FPGA configuration tool (either ChipScope™ Pro tool or Impact software), which is then used to configure the two FPGAs on the ML631 board.

The FPGAs can also be configured through the System ACE controller by setting the 3-bit configuration address DIP switches (SW3) to select one of eight bitstreams stored on a CompactFlash memory card plugged into socket U46 (see Configuration Address DIP Switches, page 16).

Upon power-on, the System ACE controller checks for the presence of a CompactFlash card and loads the FPGA configuration files from it, if present.

The JTAG chain of the board is illustrated in Figure 1-5. Each component (except the System ACE controller IC) with a JTAG interface has a bypass shunt which permits the component to be in the chain or bypassed.

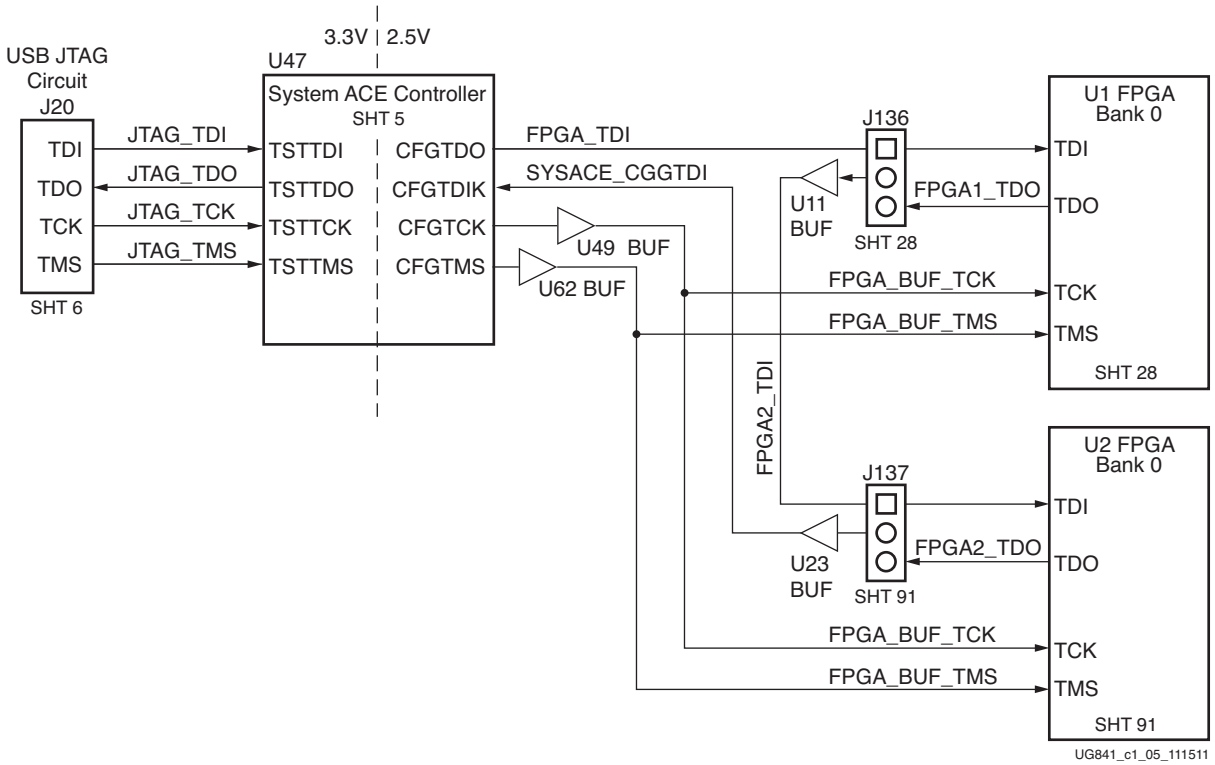

Figure 1-5: **JTAG Chain Diagram**

System ACE Controller

See Figure 1-2 callout [21].

The onboard System ACE controller (U47) allows storage of multiple configuration files on a CompactFlash card. These configuration files can be used to program the FPGAs. The CompactFlash card plugs into the CompactFlash card socket (U46) located directly above the System ACE controller on the back side of the board.

System ACE Controller Reset

See Figure 1-2 callout [22].

Pressing pushbutton SW2 (RESET) resets the System ACE controller. Reset is an active-Low input.

Configuration Address DIP Switches

See Figure 1-2 callout [23].

DIP switch SW3 selects one of the eight configuration bitstream addresses in the CompactFlash memory card. The switch settings for selecting each address are shown in Table 1-3.

Table 1-3: **SW3 DIP Switch Configuration**

Address	ADR2	ADR1	ADR0
0	O(1)	O	O
1	O	O	C(2)
2	O	C	O
3	O	C	C
4	C	O	O
5	C	O	C
6	C	C	O
7	C	C	C

Notes:

1. O indicates the open switch position (Logic 0).
2. C indicates the closed switch position (Logic 1).

More information on the System ACE controller is available in DS080, *System ACE CompactFlash Solution* [Ref 2].

U1 FPGA PROG Pushbutton, INIT LED, and DONE LED

See Figure 1-2 callout [24].

Pressing the U1 PROG pushbutton (SW5) grounds the active-Low program pin of the FPGA. The INIT LED (DS20) lights during FPGA initialization. The DONE LED (DS56) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, the DONE LED lights, indicating that the FPGA is successfully configured.

U1 FPGA User LEDs and Pushbuttons

User LEDs

See Figure 1-2 callout [25].

DS14 through DS17 are four active-High LEDs that are connected to user I/O pins on the U1 FPGA as shown in Table 1-4. These LEDs can be used to indicate status or any other purpose determined by the user.

Table 1-4: **U1 FPGA User LEDs**

U1 FPGA Pin Number	Net Name	Reference Designator
K25	U1_USER_LED1	DS17
N23	U1_USER_LED2	DS16
D21	U1_USER_LED3	DS15
K22	U1_USER_LED4	DS14

User Pushbuttons

See Figure 1-2 callout [28].

SW4, SW6, SW8, and SW9 are active-High user pushbuttons that are connected to user I/O pins on the U1 FPGA as shown in Table 1-5. These switches can be used for any purpose determined by the user.

Table 1-5: **U1 FPGA User Pushbuttons**

U1 FPGA Pin Number	Net Name	Reference Designator
H34	U1_USER_PB1	SW6
H26	U1_USER_PB2	SW4
J25	U1_USER_PB3	SW8
AR18	U1_USER_PB4	SW9

U1 FPGA 200-MHz 2.5V LVDS Oscillator

See Figure 1-2 callout [26].

The ML631 board has one 2.5V LVDS differential 200-MHz oscillator for each FPGA (SiTime Si9102AI). Oscillator U22 (located on the back side of the board) is connected to the U1 FPGA. A 100Ω terminating resistor on the PCB enables use of DIFF_SSTL15 clock buffer inside the FPGA. Table 1-6 lists the FPGA pin connections to the oscillator.

Table 1-6: **U1 FPGA LVDS Oscillator U22 Global Clock Connections (1)**

FPGA Pin Number	Net Name	U7 Pin Number
R31	U1_LVDS_OSC_P	4
R32	U1_LVDS_OSC_N	5

Notes:

1. The UCF net names for these two clock signals are CLK200_P and CLK200_N, as shown in Appendix B, ML631 Master UCF Listing for U1.

For more information on the SiTime SI9102AI oscillator, visit the SiTime website [Ref 20].

U2 FPGA PROG Pushbutton, INIT LED, and DONE LED

See Figure 1-2 callout [27].

Pressing the U2 PROG pushbutton (SW11) grounds the active-Low program pin of the FPGA. The INIT LED (DS54) lights during FPGA initialization. The DONE LED (DS29) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, the DONE LED lights, indicating that the FPGA is successfully configured.

U2 FPGA User LEDs and Pushbuttons

User LEDs

See Figure 1-2 callout [28].

D30 through D35 are six active-High LEDs that are connected to user I/O pins on U2 FPGA as shown in Table 1-7. These LEDs can be used to indicate status or any other purpose determined by the user.

Table 1-7: **U2 FPGA User LEDs**

U2 FPGA Pin	Net Name	Reference Designator
BA15	U2_USER_LED1	DS30
AY15	U2_USER_LED2	DS31
AN21	U2_USER_LED3	DS32
AM21	U2_USER_LED4	DS33
BA13	U2_USER_LED5	DS34
BA14	U2_USER_LED6	DS35

User Pushbuttons

See Figure 1-2 callout [28].

SW12, SW13, SW14, and SW15 are active-High user pushbuttons that are connected to user I/O pins on the U1 FPGA as shown in Table 1-8. These switches can be used for any purpose determined by the user.

Table 1-8: **U2 FPGA User Pushbuttons**

U2 FPGA Pin	Net Name	Reference Designator
BD18	U2_USER_PB1	SW15
BC18	U2_USER_PB2	SW12
BC14	U2_USER_PB3	SW13
BB14	U2_USER_PB4	SW14

U2 FPGA USB-to-UART Bridge

See Figure 1-2 callout [24].

Communications between the ML631 board and a host computer are through a USB cable connected to J106. Control is provided by U79, a USB-to-UART bridge (Silicon Laboratories CP2103) [Ref 21]. Table 1-9 lists the pin assignments and signals for the USB connector J106.

Table 1-9: **J106 USB Mini-B Connector Pin Assignments and Signals**

J106 Pin	Signal Name	Description
1	VBUS	+5V from host system
2	U2_USB_D_N	Bidirectional differential serial data (N-side)
3	U2_USB_D_P	Bidirectional differential serial data (P-side)
4	ID	Not used

The CP2103 supports an I/O voltage range of 2.5V on the ML631 board. The 2.5V CP2103 I/O are routed through 2.5V-to-1.5V level-shifters to provide 1.5V compatibility with U2

1.5V V_{CCO} bank 20. UART IP (for example, Xilinx XPS UART Lite) must be implemented in the FPGA logic. U2 FPGA bank 20 supports the USB-to-UART bridge using four signal pins. Connections of these signals between the FPGA and the CP2103 at U79 are listed in Table 1-10.

Table 1-10: **U2 FPGA to U79 CP2103 Bridge Connections**

U2 FPGA Pin Number	FPGA Function	Net Name	U79 Pin Number	U79 Function
AT20	Request to Send (RTS), output	U2_USB_CTS_I	22	CTS, input
AU20	Clear to Send (CTS), input	U2_USB_RTS_O	23	RTS, output
AP23	Transmit (TX), data out	U1_USB_RXD_I	24	RXD, data in
AR23	Receive (RX), data in	U1_USB_TXD_O	25	TXD, data out

A royalty-free software driver named Virtual COM Port (VCP) is available from Silicon Laboratories. This driver permits the CP2103 USB-to-UART bridge to appear as a COM port to the host computer communications application software (for example, HyperTerminal or TeraTerm). The VCP driver must be installed on the host computer prior to establishing communications with the ML631 board.

More information on the Silicon Labs CP2103 USB-to-UART bridge is available at the Silicon Labs website [Ref 21].

U2 FPGA 200-MHz 2.5V LVDS Oscillator

See Figure 1-2 callout [30].

Oscillator U63, located on the back side of the board, is connected to the U2 FPGA global clock inputs. A 100Ω terminating resistor on the PCB enables use of DIFF_SSTL15 clock buffer inside the FPGA. Table 1-11 lists the U2 FPGA pin connections to the LVDS oscillator U63.

Table 1-11: **U2 FPGA LVDS Oscillator U63 Global Clock Connections**

U2 FPGA Pin Number	Net Name	U63 Pin Number
R31	U2_LVDS_OSC_P	4
R32	U2_LVDS_OSC_N	5

More information on the SiTime SI9102AI oscillator is available at the SiTime website [Ref 20].

U1 FPGA FCI Airmax Interlaken Connectors

See Figure 1-2 callout [31, 32].

The ML631 board provides three sets of FCI Airmax male/female (plug/receptacle) connector pairs, two sets implementing the Interlaken protocol, and one set available for OTN/OTN interface [Ref 23].

Two sets of connector pins (P1/J1, P2/J2) are wired to the U1 FPGA. Table 1-12 through Table 1-17 show the U1 FPGA to FCI connector details. Refer to the block diagram in the *ML631 Schematic* for an overview of the connectivity shown in these tables [Ref 1]. U1 FPGA banks 113, 114, and 115 connect to FCI connectors P1 and J1.

Table 1-12: **U1 FPGA FCI Connector P1**

FCI Connector P1		Net Name	U1 FPGA Pin Number
Pin Name	Pin Number		
TX0_P	A7	U1_MGTTX0_115_P	AA3
TX0_N	B7	U1_MGTTX0_115_N	AA4
TX1_P	D6	U1_MGTTX1_115_P	Y1
TX1_N	E6	U1_MGTTX1_115_N	Y2
TX2_P	D8	U1_MGTTX2_115_P	W3
TX2_N	E8	U1_MGTTX2_115_N	W4
TX3_P	A9	U1_MGTTX3_115_P	V1
TX3_N	B9	U1_MGTTX3_115_N	V2
TX4_P	A3	U1_MGTTX1_114_P	AD1
TX4_N	B3	U1_MGTTX1_114_N	AD2
TX5_P	D2	U1_MGTTX0_114_P	AE3
TX5_N	E2	U1_MGTTX0_114_N	AE4
TX6_P	D4	U1_MGTTX2_114_P	AC3
TX6_N	E4	U1_MGTTX2_114_N	AC4
TX7_P	A5	U1_MGTTX3_114_P	AB1
TX7_N	B5	U1_MGTTX3_114_N	AB2
TX_REFCLK_P	A1	U1_P1_TX_REFCLK_C_P	U13.16
TX_REFCLK_N	B1	U1_P1_TX_REFCLK_C_N	U13.17
TX_FC_CK	E10	U1_AMH1_FC_CK	BD33
TX8_P	G5	U1_MGTTX3_113_P	AF1
TX8_N	H5	U1_MGTTX3_113_N	AF2
TX9_P	G3	U1_MGTTX1_113_P	AH1
TX9_N	H3	U1_MGTTX1_113_N	AH2
TX10_P	J4	U1_MGTTX2_113_P	AG3
TX10_N	K4	U1_MGTTX2_113_N	AG4
TX11_P	G1	U1_MGTTX0_113_P	AJ3
TX11_N	H1	U1_MGTTX0_113_N	AJ4
TX12_P	J6	U1_AMH1_IO0	BB24
TX12_N	K6	U1_AMH1_IO1	BA24
TX13_P	J10	U1_AMH1_IO2	AP24
TX13_N	K10	U1_AMH1_IO3	AN24
TX14_P	J2	U1_AMH1_IO4	AU24

Table 1-12: **U1 FPGA FCI Connector P1 *(Cont'd)***

FCI Connector P1		Net Name	U1 FPGA Pin Number
Pin Name	Pin Number		
TX14_N	K2	U1_AMH1_IO5	AR25
TX15_P	J8	U1_AMH1_IO6	AP25
TX15_N	K8	U1_AMH1_IO7	AJ18
TX_FC_DATA	H7	U1_AMH1_FC_DATA	BC33
TX_FC_SYNC	H9	U1_AMH1_FC_SYNC	AL33

Table 1-13: **U1 FPGA FCI Connector J1**

FCI Connector J1		Net Name	U1 FPGA Pin Number
Pin Name	Pin Number		
RX0_P	A7	U1_MGTRX0_115_C_P	Y5
RX0_N	B7	U1_MGTRX0_115_C_N	Y6
RX1_P	D6	U1_MGTRX1_115_C_P	W7
RX1_N	E6	U1_MGTRX1_115_C_N	W8
RX2_P	D8	U1_MGTRX2_115_C_P	V5
RX2_N	E8	U1_MGTRX2_115_C_N	V6
RX3_P	A9	U1_MGTRX3_115_C_P	U7
RX3_N	B9	U1_MGTRX3_115_C_N	U8
RX4_P	A3	U1_MGTRX1_114_C_P	AC7
RX4_N	B3	U1_MGTRX1_114_C_N	AC8
RX5_P	D2	U1_MGTRX0_114_C_P	AD5
RX5_N	E2	U1_MGTRX0_114_C_N	AD6
RX6_P	D4	U1_MGTRX2_114_C_P	AB5
RX6_N	E4	U1_MGTRX2_114_C_N	AB6
RX7_P	A5	U1_MGTRX3_114_C_P	AA7
RX7_N	B5	U1_MGTRX3_114_C_N	AA8
RX_REFCLK_P	A1	U1_J1_RX_REFCLK_P	Y10
RX_REFCLK_N	B1	U1_J1_RX_REFCLK_N	Y9
RX_FC_CK	E10	U1_AMR1_FC_CK	AK32
RX8_P	G5	U1_MGTRX3_113_C_P	AE7
RX8_N	H5	U1_MGTRX3_113_C_N	AE8
RX9_P	G3	U1_MGTRX1_113_C_P	AG7
RX9_N	H3	U1_MGTRX1_113_C_N	AG8

Table 1-13: **U1 FPGA FCI Connector J1 *(Cont'd)***

FCI Connector J1		Net Name	U1 FPGA Pin Number
Pin Name	Pin Number		
RX10_P	J4	U1_MGTRX2_113_C_P	AF5
RX10_N	K4	U1_MGTRX2_113_C_N	AF6
RX11_P	G1	U1_MGTRX0_113_C_P	AH5
RX11_N	H1	U1_MGTRX0_113_C_N	AH6
RX12_P	J6	NC	
RX12_N	K6	NC	
RX13_P	J10	NC	
RX13_N	K10	NC	
RX14_P	J2	NC	
RX14_N	K2	NC	
RX15_P	J8	NC	
RX15_N	K8	NC	
RX_FC_DATA	H7	U1_AMR1_FC_DATA	BA34
RX_FC_SYNC	H9	U1_AMR1_FC_SYNC	AL34

Table 1-14: **U1 FPGA FCI Connector P2**

FCI Connector P2		Net Names	U1 FPGA Pin Number
Pin Names	Pin Number		
TX0_P	A7	U1_MGTTX1_101_P	AT44
TX0_N	B7	U1_MGTTX1_101_N	AT43
TX1_P	D6	U1_MGTTX0_101_P	AU42
TX1_N	E6	U1_MGTTX0_101_N	AU41
TX2_P	D8	U1_MGTTX2_101_P	AR42
TX2_N	E8	U1_MGTTX2_101_N	AR41
TX3_P	A9	U1_MGTTX3_101_P	AP44
TX3_N	B9	U1_MGTTX3_101_N	AP43
TX4_P	A3	U1_MGTTX0_100_P	BB44
TX4_N	B3	U1_MGTTX0_100_N	BB43
TX5_P	D2	U1_MGTTX2_100_P	AW42
TX5_N	E2	U1_MGTTX2_100_N	AW41
TX6_P	D4	U1_MGTTX1_100_P	AY44
TX6_N	E4	U1_MGTTX1_100_N	AY43

Table 1-14: **U1 FPGA FCI Connector P2 *(Cont'd)***

FCI Connector P2		Net Names	U1 FPGA Pin Number
Pin Names	Pin Number		
TX7_P	A5	U1_MGTTX3_100_P	AV44
TX7_N	B5	U1_MGTTX3_100_N	AV43
TX_REFCLK_P	A1	U1_P2_TX_REFCLK_C_P	U13.19
TX_REFCLK_N	B1	U1_P2_TX_REFCLK_C_N	U13.20
TX_FC_CK	E10	U1_AMH2_FC_CK	J30
TX8_P	G5	U1_MGTTX2_102_P	AL42
TX8_N	H5	U1_MGTTX2_102_N	AL41
TX9_P	G3	U1_MGTTX0_102_P	AN42
TX9_N	H3	U1_MGTTX0_102_N	AN41
TX10_P	J4	U1_MGTTX3_102_P	AK44
TX10_N	K4	U1_MGTTX3_102_N	AK43
TX11_P	G1	U1_MGTTX1_102_P	AM44
TX11_N	H1	U1_MGTTX1_102_N	AM43
TX12_P	J6	U1_AMH2_IO0	AV21
TX12_N	K6	U1_AMH2_IO1	AU21
TX13_P	J10	U1_AMH2_IO2	AN22
TX13_N	K10	U1_AMH2_IO3	AN23
TX14_P	J2	U1_AMH2_IO4	AY21
TX14_N	K2	U1_AMH2_IO5	AU20
TX15_P	J8	U1_AMH2_IO6	AT20
TX15_N	K8	U1_AMH2_IO7	AP21
TX_FC_DATA	H7	U1_AMH2_FC_DATA	K30
TX_FC_SYNC	H9	U1_AMH2_FC_SYNC	T30

Table 1-15: **U1 FPGA FCI Connector J2**

FCI Connector J2		Net Names	U1 FPGA Pin Number
Pin Names	Pin Number		
RX0_P	A7	U1_MGTRX1_101_C_P	AV40
RX0_N	B7	U1_MGTRX1_101_C_N	AV39
RX1_P	D6	U1_MGTRX0_101_C_P	AY40
RX1_N	E6	U1_MGTRX0_101_C_N	AY39
RX2_P	D8	U1_MGTRX2_101_C_P	AT40

Table 1-15: **U1 FPGA FCI Connector J2 *(Cont'd)***

FCI Connector J2		Net Names	U1 FPGA Pin Number
Pin Names	Pin Number		
RX2_N	E8	U1_MGTRX2_101_C_N	AT39
RX3_P	A9	U1_MGTRX3_101_C_P	AP40
RX3_N	B9	U1_MGTRX3_101_C_N	AP39
RX4_P	A3	U1_MGTRX0_100_C_P	BD40
RX4_N	B3	U1_MGTRX0_100_C_N	BD39
RX5_P	D2	U1_MGTRX2_100_C_P	BB40
RX5_N	E2	U1_MGTRX2_100_C_N	BB39
RX6_P	D4	U1_MGTRX1_100_C_P	BC42
RX6_N	E4	U1_MGTRX1_100_C_N	BC41
RX7_P	A5	U1_MGTRX3_100_C_P	BA42
RX7_N	B5	U1_MGTRX3_100_C_N	BA41
RX_REFCLK_P	A1	U1_J2_RX_REFCLK_P	AR37
RX_REFCLK_N	B1	U1_J2_RX_REFCLK_N	AR38
RX_FC_CK	E10	U1_AMR2_FC_CK	T29
RX8_P	G5	U1_MGTRX2_102_C_P	AJ38
RX8_N	H5	U1_MGTRX2_102_C_N	AJ37
RX9_P	G3	U1_MGTRX0_102_C_P	AL38
RX9_N	H3	U1_MGTRX0_102_C_N	AL37
RX10_P	J4	U1_MGTRX3_102_C_P	AK40
RX10_N	K4	U1_MGTRX3_102_C_N	AK39
RX11_P	G1	U1_MGTRX1_102_C_P	AM40
RX11_N	H1	U1_MGTRX1_102_C_N	AM39
RX12_P	J6	NC	
RX12_N	K6	NC	
RX13_P	J10	NC	
RX13_N	K10	NC	
RX14_P	J2	NC	
RX14_N	K2	NC	
RX15_P	J8	NC	
RX15_N	K8	NC	
RX_FC_DATA	H7	U1_AMR2_FC_DATA	G32
RX_FC_SYNC	H9	U1_AMR2_FC_SYNC	M32

U2 FPGA FCI Airmax OTN/OTN Client Connectors

See Figure 1-2 callout [33].

Table 1-16 and Table 1-17 show the U2 FPGA GTH transceiver Quads 106, 107, and 108 to FCI connector P4/J4 connection details. Refer to the block diagram in the *ML631 Schematic* for an overview of the connectivity shown [Ref 1].

Table 1-16: **U2 FPGA FCI Connector P4**

FCI Connector P4		Net Name	U2 FPGA Pin Number
Pin Name	Pin Number		
TX0_P	A7	U2_MGTTX2_106_P	M43
TX0_N	B7	U2_MGTTX2_106_N	M44
TX1_P	D6	U2_MGTTX3_106_P	N41
TX1_N	E6	U2_MGTTX3_106_N	N42
TX2_P	D8	U2_MGTTX1_106_P	P43
TX2_N	E8	U2_MGTTX1_106_N	P44
TX3_P	A9	U2_MGTTX0_106_P	T43
TX3_N	B9	U2_MGTTX0_106_N	T44
TX4_P	A3	U2_MGTTX1_108_P	D43
TX4_N	B3	U2_MGTTX1_108_N	D44
TX5_P	D2	U2_MGTTX3_108_P	C41
TX5_N	E2	U2_MGTTX3_108_N	C42
TX6_P	D4	U2_MGTTX2_107_P	G41
TX6_N	E4	U2_MGTTX2_107_N	G42
TX7_P	A5	U2_MGTTX0_107_P	L41
TX7_N	B5	U2_MGTTX0_107_N	L42
TX_REFCLK_P	A1	U2_P4_TX_REFCLK_C_P	U18.19
TX_REFCLK_N	B1	U2_P4_TX_REFCLK_C_N	U18.20
TX_FC_CK	E10	U2_AMH4_FC_CK	BB24
TX8_P	G5	U2_MGTTX1_107_P	K43
TX8_N	H5	U2_MGTTX1_107_N	K44
TX9_P	G3	U2_MGTTX0_108_P	F43
TX9_N	H3	U2_MGTTX0_108_N	F44
TX10_P	J4	U2_MGTTX3_107_P	H43
TX10_N	K4	U2_MGTTX3_107_N	H44
TX11_P	G1	U2_MGTTX2_108_P	A41
TX11_N	H1	U2_MGTTX2_108_N	A42

Table 1-16: **U2 FPGA FCI Connector P4 *(Cont'd)***

FCI Connector P4		Net Name	U2 FPGA Pin Number
Pin Name	Pin Number		
TX12_P	J6	U2_AMH4_IO0	AV21
TX12_N	K6	U2_AMH4_IO1	AU21
TX13_P	J10	U2_AMH4_IO2	AN22
TX13_N	K10	U2_AMH4_IO3	AN23
TX14_P	J2	U2_AMH4_IO4	AY21
TX14_N	K2	U2_AMH4_IO5	AW21
TX15_P	J8	U2_AMH4_IO6	AW23
TX15_N	K8	U2_AMH4_IO7	AV23
TX_FC_DATA	H7	U2_AMH4_FC_DATA	BA24
TX_FC_SYNC	H9	U2_AMH4_FC_SYNC	AP24

Table 1-17: **U2 FPGA FCI Connector J4**

FCI Connector J4		Net Name	U2 FPGA Pin Number
Pin Name	Pin Number		
RX0_P	A7	U2_MGTRX2_106_C_P	N37
RX0_N	B7	U2_MGTRX2_106_C_N	N38
RX1_P	D6	U2_MGTRX3_106_C_P	M39
RX1_N	E6	U2_MGTRX3_106_C_N	M40
RX2_P	D8	U2_MGTRX1_106_C_P	T39
RX2_N	E8	U2_MGTRX1_106_C_N	T40
RX3_P	A9	U2_MGTRX0_106_C_P	U41
RX3_N	B9	U2_MGTRX0_106_C_N	U42
RX4_P	A3	U2_MGTRX1_108_C_P	F39
RX4_N	B3	U2_MGTRX1_108_C_N	F40
RX5_P	D2	U2_MGTRX3_108_C_P	D39
RX5_N	E2	U2_MGTRX3_108_C_N	D40
RX6_P	D4	U2_MGTRX2_107_C_P	H39
RX6_N	E4	U2_MGTRX2_107_C_N	H40
RX7_P	A5	U2_MGTRX0_107_C_P	K39
RX7_N	B5	U2_MGTRX0_107_C_N	K40
RX_REFCLK_P	A1	U2_J4_RX_REFCLK_P	SMA J134
RX_REFCLK_N	B1	U2_J4_RX_REFCLK_N	SMA J135

Table 1-17: **U2 FPGA FCI Connector J4 *(Cont'd)***

FCI Connector J4		Net Name	U2 FPGA Pin Number
Pin Name	Pin Number		
RX_FC_CK	E10	U2_AMR4_FC_CK	AN24
RX8_P	G5	U2_MGTRX1_107_C_P	L37
RX8_N	H5	U2_MGTRX1_107_C_N	L38
RX9_P	G3	U2_MGTRX0_108_C_P	G37
RX9_N	H3	U2_MGTRX0_108_C_N	G38
RX10_P	J4	U2_MGTRX3_107_C_P	J37
RX10_N	K4	U2_MGTRX3_107_C_N	J38
RX11_P	G1	U2_MGTRX2_108_C_P	B39
RX11_N	H1	U2_MGTRX2_108_C_N	B40
RX12_P	J6	NC	
RX12_N	K6	NC	
RX13_P	J10	NC	
RX13_N	K10	NC	
RX14_P	J2	NC	
RX14_N	K2	NC	
RX15_P	J8	NC	
RX15_N	K8	NC	
RX_FC_DATA	H7	U2_AMR4_FC_DATA	AU24
RX_FC_SYNC	H9	U2_AMR4_FC_SYNC	AT24

U2 FPGA FCI Connector J4 RX Reference Clock

See Figure 1-2 callout [34].

The J4 FCI Airmax receptacle RX reference clock is wired to the SMA pair J134 and J135 as shown in Table 1-18.

Table 1-18: **FCI J4 RX Reference Clock to SMA Connection**

FCI Connector J4		Net Name	SMA Connection SMA Pin Number
Pin Name	Pin Number		
RX_REFCLK_P	A1	U2_J4_RX_REFCLK_P	J134.1
RX_REFCLK_N	B1	U2_J4_RX_REFCLK_N	J135.1

U1 FPGA GTX Transceiver to U2 FPGA GTX Transceiver Interface

See Figure 1-2 callout [1, 2].

ML631 board FPGAs implement four GTX transceiver direct U1 to U2 connections. The U1 FPGA GTX transceiver Quads 103 through 105 and 112 are wired directly to U2 FPGA GTX transceiver Quads 113 through 115 and 112, respectively. Figure 1-6 and Table 1-19 through Table 1-22 show details of this U1 to U2 GTX transceiver interconnectivity. GTH transceiver connectivity is discussed in the next section.

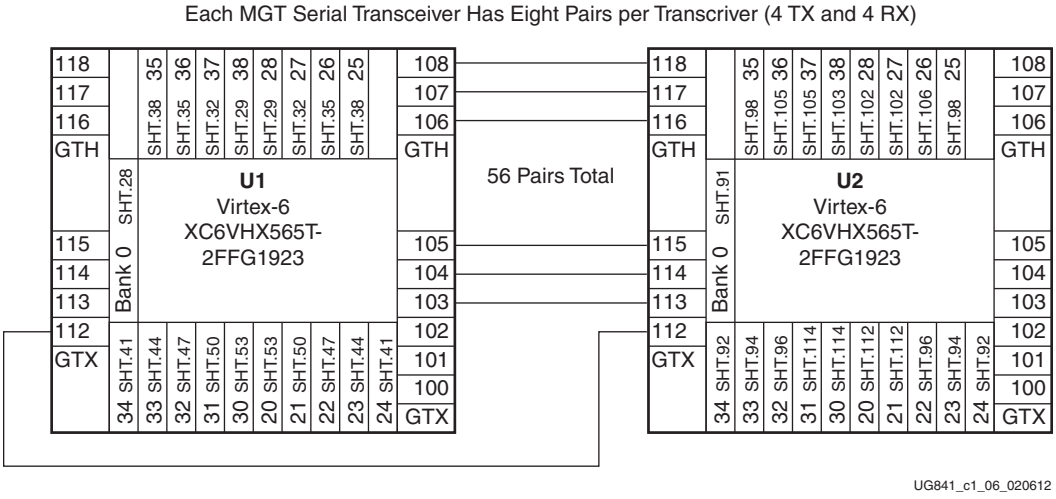

Figure 1-6: **U1 to U2 MGT GTX Transceiver and GTH Transceiver Direct Connections**

Table 1-19: **U1 FPGA GTX103 to U2 FPGA GTX113 Connections**

U1 FPGA GTX103 Quad		Net Name	U2 FPGA GTX113 Quad	
Pin Name	Pin Number		Pin Number	Pin Name
MGTTXP0_103_AJ42	AJ42	U1_MGTTX0_103_P	AH5	MGTRXP0_113_AH5
MGTTXN0_103_AJ41	AJ41	U1_MGTTX0_103_N	AH6	MGTRXN0_113_AH6
MGTRXP0_103_AH40	AH40	U2_MGTTX0_113_P	AJ3	MGTTXP0_113_AJ3

Table 1-19: **U1 FPGA GTX103 to U2 FPGA GTX113 Connections *(Cont'd)***

U1 FPGA GTX103 Quad		Net Name	U2 FPGA GTX113 Quad	
Pin Name	Pin Number		Pin Number	Pin Name
MGTRXN0_103_AH39	AH39	U2_MGTTX0_113_N	AJ4	MGTTXN0_113_AJ4
MGTTXP1_103_AH44	AH44	U1_MGTTX1_103_P	AG7	MGTRXP1_113_AG7
MGTTXN1_103_AH43	AH43	U1_MGTTX1_103_N	AG8	MGTRXN1_113_AG8
MGTRXP1_103_AG38	AG38	U2_MGTTX1_113_P	AH1	MGTTXP1_113_AH1
MGTRXN1_103_AG37	AG37	U2_MGTTX1_113_N	AH2	MGTTXN1_113_AH2
MGTTXP2_103_AG42	AG42	U1_MGTTX2_103_P	AF5	MGTRXP2_113_AF5
MGTTXN2_103_AG41	AG41	U1_MGTTX2_103_N	AF6	MGTRXN2_113_AF6
MGTRXP2_103_AF40	AF40	U2_MGTTX2_113_P	AG3	MGTTXP2_113_AG3
MGTRXN2_103_AF39	AF39	U2_MGTTX2_113_N	AG4	MGTTXN2_113_AG4
MGTTXP3_103_AF44	AF44	U1_MGTTX3_103_P	AE7	MGTRXP3_113_AE7
MGTTXN3_103_AF43	AF43	U1_MGTTX3_103_N	AE8	MGTRXN3_113_AE8
MGTRXP3_103_AE38	AE38	U2_MGTTX3_113_P	AF1	MGTTXP3_113_AF1
MGTRXN3_103_AE37	AE37	U2_MGTTX3_113_N	AF2	MGTTXN3_113_AF2
MGTREFCLK0P_103_AF35	AF35	NC	AF10	MGTREFCLK0P_113_AF10
MGTREFCLK0N_103_AF36	AF36	NC	AF9	MGTREFCLK0N_113_AF9
MGTREFCLK1P_103_AD35	AD35	NC	AD10	MGTREFCLK1P_113_AD10
MGTREFCLK1N_103_AD36	AD36	NC	AD9	MGTREFCLK1N_113_AD9

Table 1-20: **U1 FPGA GTX104 to U2 FPGA GTX114 Connections**

U1 FPGA GTX104 Quad		Net Name	U2 FPGA GTX114 Quad	
Pin Name	Pin Number		Pin Number	Pin Name
MGTTXP0_104_AE42	AE42	U1_MGTTX0_104_P	AD5	MGTRXP0_114_AD5
MGTTXN0_104_AE41	AE41	U1_MGTTX0_104_N	AD6	MGTRXN0_114_AD6
MGTRXP0_104_AD40	AD40	U2_MGTTX0_114_P	AE3	MGTTXP0_114_AE3
MGTRXN0_104_AD39	AD39	U2_MGTTX0_114_N	AE4	MGTTXN0_114_AE4
MGTTXP1_104_AD44	AD44	U1_MGTTX1_104_P	AC7	MGTRXP1_114_AC7
MGTTXN1_104_AD43	AD43	U1_MGTTX1_104_N	AC8	MGTRXN1_114_AC8
MGTRXP1_104_AC38	AC38	U2_MGTTX1_114_P	AD1	MGTTXP1_114_AD1
MGTRXN1_104_AC37	AC37	U2_MGTTX1_114_N	AD2	MGTTXN1_114_AD2
MGTTXP2_104_AC42	AC42	U1_MGTTX2_104_P	AB5	MGTRXP2_114_AB5
MGTTXN2_104_AC41	AC41	U1_MGTTX2_104_N	AB6	MGTRXN2_114_AB6
MGTRXP2_104_AB40	AB40	U2_MGTTX2_114_P	AC3	MGTTXP2_114_AC3

Table 1-20: **U1 FPGA GTX104 to U2 FPGA GTX114 Connections *(Cont'd)***

U1 FPGA GTX104 Quad		Net Name		U2 FPGA GTX114 Quad	
Pin Name	**Pin Number**			**Pin Number**	**Pin Name**
MGTRXN2_104_AB39	AB39	U2_MGTTX2_114_N		AC4	MGTTXN2_114_AC4
MGTTXP3_104_AB44	AB44	U1_MGTTX3_104_P		AA7	MGTRXP3_114_AA7
MGTTXN3_104_AB43	AB43	U1_MGTTX3_104_N		AA8	MGTRXN3_114_AA8
MGTRXP3_104_AA38	AA38	U2_MGTTX3_114_P		AB1	MGTTXP3_114_AB1
MGTRXN3_104_AA37	AA37	U2_MGTTX3_114_N		AB2	MGTTXN3_114_AB2
Clock Source					
MGTREFCLK0P_104_AB35	AB35	U114.1	U114.3	AB10	MGTREFCLK0P_114_AB10
MGTREFCLK0N_104_AB36	AB36	U114.2	U114.4	AB9	MGTREFCLK0N_114_AB9
MGTREFCLK1P_104_Y35	Y35	U13.11	U13.13	Y10	MGTREFCLK1P_114_Y10
MGTREFCLK1N_104_Y36	Y36	U13.12	U13.14	Y9	MGTREFCLK1N_114_Y9

Table 1-21: **U1 FPGA GTX105 to U2 FPGA GTX115 Connections**

U1 FPGA GTX105 Quad		Net Name	U2 FPGA GTX115 Quad	
Pin Name	**Pin Number**		**Pin Number**	**Pin Name**
MGTTXP0_105_AA42	AA42	U1_MGTTX0_105_P	Y5	MGTRXP0_115_Y5
MGTTXN0_105_AA41	AA41	U1_MGTTX0_105_N	Y6	MGTRXN0_115_Y6
MGTRXP0_105_Y40	Y40	U2_MGTTX0_115_P	AA3	MGTTXP0_115_AA3
MGTRXN0_105_Y39	Y39	U2_MGTTX0_115_N	AA4	MGTTXN0_115_AA4
MGTTXP1_105_Y44	Y44	U1_MGTTX1_105_P	W7	MGTRXP1_115_W7
MGTTXN1_105_Y43	Y43	U1_MGTTX1_105_N	W8	MGTRXN1_115_W8
MGTRXP1_105_W38	W38	U2_MGTTX1_115_P	Y1	MGTTXP1_115_Y1
MGTRXN1_105_W37	W37	U2_MGTTX1_115_N	Y2	MGTTXN1_115_Y2
MGTTXP2_105_W42	W42	U1_MGTTX2_105_P	V5	MGTRXP2_115_V5
MGTTXN2_105_W41	W41	U1_MGTTX2_105_N	V6	MGTRXN2_115_V6
MGTRXP2_105_V40	V40	U2_MGTTX2_115_P	W3	MGTTXP2_115_W3
MGTRXN2_105_V39	V39	U2_MGTTX2_115_N	W4	MGTTXN2_115_W4
MGTTXP3_105_V44	V44	U1_MGTTX3_105_P	U7	MGTRXP3_115_U7
MGTTXN3_105_V43	V43	U1_MGTTX3_105_N	U8	MGTRXN3_115_U8
MGTRXP3_105_U38	U38	U2_MGTTX3_115_P	V1	MGTTXP3_115_V1
MGTRXN3_105_U37	U37	U2_MGTTX3_115_N	V2	MGTTXN3_115_V2
MGTREFCLK0P_105_V35	V35	NC	V10	MGTREFCLK0P_115_V10
MGTREFCLK0N_105_V36	V36	NC	V9	MGTREFCLK0N_115_V9

Table 1-21: **U1 FPGA GTX105 to U2 FPGA GTX115 Connections *(Cont'd)***

U1 FPGA GTX105 Quad		Net Name	U2 FPGA GTX115 Quad	
Pin Name	Pin Number		Pin Number	Pin Name
MGTREFCLK1P_105_T35	T35	NC	T10	MGTREFCLK1P_115_T10
MGTREFCLK1N_105_T36	T36	NC	T9	MGTREFCLK1N_115_T9

Table 1-22: **U1 FPGA GTX112 to U2 FPGA GTX112 Connections**

U1 FPGA GTX112 Quad		Net Name		U2 FPGA GTX112 Quad	
Pin Name	Pin Number			Pin Number	Pin Name
MGTTXP0_112_AN3	AN3	U1_MGTTX0_112_P		AL7	MGTRXP0_112_AL7
MGTTXN0_112_AN4	AN4	U1_MGTTX0_112_N		AL8	MGTRXN0_112_AL8
MGTRXP0_112_AL7	AL7	U2_MGTTX0_112_P		AN3	MGTTXP0_112_AN3
MGTRXN0_112_AL8	AL8	U2_MGTTX0_112_N		AN4	MGTTXN0_112_AN4
MGTTXP1_112_AM1	AM1	U1_MGTTX1_112_P		AM5	MGTRXP1_112_AM5
MGTTXN1_112_AM2	AM2	U1_MGTTX1_112_N		AM6	MGTRXN1_112_AM6
MGTRXP1_112_AM5	AM5	U2_MGTTX1_112_P		AM1	MGTTXP1_112_AM1
MGTRXN1_112_AM6	AM6	U2_MGTTX1_112_N		AM2	MGTTXN1_112_AM2
MGTTXP2_112_AL3	AL3	U1_MGTTX2_112_P		AJ7	MGTRXP2_112_AJ7
MGTTXN2_112_AL4	AL4	U1_MGTTX2_112_N		AJ8	MGTRXN2_112_AJ8
MGTRXP2_112_AJ7	AJ7	U2_MGTTX2_112_P		AL3	MGTTXP2_112_AL3
MGTRXN2_112_AJ8	AJ8	U2_MGTTX2_112_N		AL4	MGTTXN2_112_AL4
MGTTXP3_112_AK1	AK1	U1_MGTTX3_112_P		AK5	MGTRXP3_112_AK5
MGTTXN3_112_AK2	AK2	U1_MGTTX3_112_N		AK6	MGTRXN3_112_AK6
MGTRXP3_112_AK5	AK5	U2_MGTTX3_112_P		AK1	MGTTXP3_112_AK1
MGTRXN3_112_AK6	AK6	U2_MGTTX3_112_N		AK2	MGTTXN3_112_AK2
Clock Source					
MGTREFCLK0P_112_AN8	AN8	U113.1	U113.3	AN8	MGTREFCLK0P_112_AN8
MGTREFCLK0N_112_AN7	AN7	U113.2	U113.4	AN7	MGTREFCLK0N_112_AN7
MGTREFCLK1P_112_AH10	AH10	U18.11	U18.13	AH10	MGTREFCLK1P_112_AH10
MGTREFCLK1N_112_AH9	AH9	U18.12	U18.14	AH9	MGTREFCLK1N_112_AH9

U1 FPGA GTH Transceiver to U2 FPGA GTH Transceiver Interface

See Figure 1-2 callout [1, 2].

The ML631 board FPGAs implement three GTH transceiver direct U1-to-U2 connections. U1 FPGA Quads GTH106 through 108 are wired directly to U2 FPGA GTH116 through 118.

Table 1-23 through Table 1-25 show details of this U1 to U2 GTH transceiver interconnectivity (see Figure 1-6).

Table 1-23: **U1 FPGA GTH106 to U2 FPGA GTH116 Connections**

U1 FPGA GTH106 Quad		Net Name		U2 FPGA GTH116 Quad	
Pin Name	Pin Number			Pin Number	Pin Name
MGTTXP0_106_T43	T43	U1_MGTTX0_106_P		U4	MGTRXP0_116_U4
MGTTXN0_106_T44	T44	U1_MGTTX0_106_N		U3	MGTRXN0_116_U3
MGTRXP0_106_U41	U41	U2_MGTTX0_116_P		T2	MGTTXP0_116_T2
MGTRXN0_106_U42	U42	U2_MGTTX0_116_N		T1	MGTTXN0_116_T1
MGTTXP1_106_P43	P43	U1_MGTTX1_106_P		T6	MGTRXP1_116_T6
MGTTXN1_106_P44	P44	U1_MGTTX1_106_N		T5	MGTRXN1_116_T5
MGTRXP1_106_T39	T39	U2_MGTTX1_116_P		P2	MGTTXP1_116_P2
MGTRXN1_106_T40	T40	U2_MGTTX1_116_N		P1	MGTTXN1_116_P1
MGTTXP2_106_M43	M43	U1_MGTTX2_106_P		N8	MGTRXP2_116_N8
MGTTXN2_106_M44	M44	U1_MGTTX2_106_N		N7	MGTRXN2_116_N7
MGTRXP2_106_N37	N37	U2_MGTTX2_116_P		M2	MGTTXP2_116_M2
MGTRXN2_106_N38	N38	U2_MGTTX2_116_N		M1	MGTTXN2_116_M1
MGTTXP3_106_N41	N41	U1_MGTTX3_106_P		M6	MGTRXP3_116_M6
MGTTXN3_106_N42	N42	U1_MGTTX3_106_N		M5	MGTRXN3_116_M5
MGTRXP3_106_M39	M39	U2_MGTTX3_116_P		N4	MGTTXP3_116_N4
MGTRXN3_106_M40	M40	U2_MGTTX3_116_N		N3	MGTTXN3_116_N3
Clock Source					
MGTREFCLKP_106_R41	R41	U102.19	U122.19	R4	MGTREFCLKP_116_R4
MGTREFCLKN_106_R42	R42	U102.18	U122.18	R3	MGTREFCLKN_116_R3

Table 1-24: **U1 FPGA GTH107 to U2 FPGA GTH117 Connections**

U1 FPGA GTH107 Quad		Net Name	U2 FPGA GTH117 Quad	
Pin Name	Pin Number		Pin Number	Pin Name
MGTTXP0_107_L41	L41	U1_MGTTX0_107_P	K6	MGTRXP0_117_K6
MGTTXN0_107_L42	L42	U1_MGTTX0_107_N	K5	MGTRXN0_117_K5
MGTRXP0_107_K39	K39	U2_MGTTX0_117_P	L4	MGTTXP0_117_L4
MGTRXN0_107_K40	K40	U2_MGTTX0_117_N	L3	MGTTXN0_117_L3
MGTTXP1_107_K43	K43	U1_MGTTX1_107_P	L8	MGTRXP1_117_L8
MGTTXN1_107_K44	K44	U1_MGTTX1_107_N	L7	MGTRXN1_117_L7
MGTRXP1_107_L37	L37	U2_MGTTX1_117_P	K2	MGTTXP1_117_K2

Table 1-24: **U1 FPGA GTH107 to U2 FPGA GTH117 Connections *(Cont'd)***

U1 FPGA GTH107 Quad		Net Name		U2 FPGA GTH117 Quad	
Pin Name	Pin Number			Pin Number	Pin Name
MGTRXN1_107_L38	L38	U2_MGTTX1_117_N		K1	MGTTXN1_117_K1
MGTTXP2_107_G41	G41	U1_MGTTX2_107_P		H6	MGTRXP2_117_H6
MGTTXN2_107_G42	G42	U1_MGTTX2_107_N		H5	MGTRXN2_117_H5
MGTRXP2_107_H39	H39	U2_MGTTX2_117_P		G4	MGTTXP2_117_G4
MGTRXN2_107_H40	H40	U2_MGTTX2_117_N		G3	MGTTXN2_117_G3
MGTTXP3_107_H43	H43	U1_MGTTX3_107_P		J8	MGTRXP3_117_J8
MGTTXN3_107_H44	H44	U1_MGTTX3_107_N		J7	MGTRXN3_117_J7
MGTRXP3_107_J37	J37	U2_MGTTX3_117_P		H2	MGTTXP3_117_H2
MGTRXN3_107_J38	J38	U2_MGTTX3_117_N		H1	MGTTXN3_117_H1
Clock Source					
MGTREFCLKP_107_J41	J41	U102.13	U122.13	J4	MGTREFCLKP_117_J4
MGTREFCLKN_107_J42	J42	U102.12	U122.12	J3	MGTREFCLKN_117_J3

Table 1-25: **U1 FPGA GTH108 to U2 FPGA GTH118 Connections**

U1 FPGA GTH108 Quad		Net Name	U2 FPGA GTH118 Quad	
Pin Name	Pin Number		Pin Number	Pin Name
MGTTXP0_108_F43	F43	U1_MGTTX0_108_P	G8	MGTRXP0_118_G8
MGTTXN0_108_F44	F44	U1_MGTTX0_108_N	G7	MGTRXN0_118_G7
MGTRXP0_108_G37	G37	U2_MGTTX0_118_P	F2	MGTTXP0_118_F2
MGTRXN0_108_G38	G38	U2_MGTTX0_118_N	F1	MGTTXN0_118_F1
MGTTXP1_108_D43	D43	U1_MGTTX1_108_P	F6	MGTRXP1_118_F6
MGTTXN1_108_D44	D44	U1_MGTTX1_108_N	F5	MGTRXN1_118_F5
MGTRXP1_108_F39	F39	U2_MGTTX1_118_P	D2	MGTTXP1_118_D2
MGTRXN1_108_F40	F40	U2_MGTTX1_118_N	D1	MGTTXN1_118_D1
MGTTXP2_108_A41	A41	U1_MGTTX2_108_P	B6	MGTRXP2_118_B6
MGTTXN2_108_A42	A42	U1_MGTTX2_108_N	B5	MGTRXN2_118_B5
MGTRXP2_108_B39	B39	U2_MGTTX2_118_P	A4	MGTTXP2_118_A4
MGTRXN2_108_B40	B40	U2_MGTTX2_118_N	A3	MGTTXN2_118_A3
MGTTXP3_108_C41	C41	U1_MGTTX3_108_P	D6	MGTRXP3_118_D6
MGTTXN3_108_C42	C42	U1_MGTTX3_108_N	D5	MGTRXN3_118_D5
MGTRXP3_108_D39	D39	U2_MGTTX3_118_P	C4	MGTTXP3_118_C4
MGTRXN3_108_D40	D40	U2_MGTTX3_118_N	C3	MGTTXN3_118_C3

Table 1-25: **U1 FPGA GTH108 to U2 FPGA GTH118 Connections *(Cont'd)***

U1 FPGA GTH108 Quad		Net Name		U2 FPGA GTH118 Quad	
Pin Name	Pin Number			Pin Number	Pin Name
Clock Source					
MGTREFCLKP_108_E41	E41	U115.19	U121.13	E4	MGTREFCLKP_118_E4
MGTREFCLKN_108_E42	E42	U115.18	U121.12	E3	MGTREFCLKN_118_E3

U1 and U2 FPGA Differential SMA Clock Inputs

See Figure 1-2 callouts [35, 36, 37, 38].

The ML631 board provides four pairs of differential input SMA connectors. Each pair is connected to a 1-to-2, 3.3V LVPECL ICS85311AMLF clock buffer. The eight clock buffer outputs have net names of CLK_DIFF_<CH#>_Q0_P/N and CLK_DIFF_<CH#>_Q1_P/N, where channel number <CH#> ranges from 0 to 3. These signal pairs connect to the four even differential inputs (0, 2, 4, and 6) on each of the two TI SN65LVCP408PAP 8 x 8 crosspoint switch ICs U57 and U58 (nets …Q0_P/N to U57 and nets …Q1_P/N to U58). Table 1-26 traces the path of the clock pair nets from the source SMA pair to the destination crosspoint switch input pins. Refer to *ML631 Schematic* pages 9 and 14 for these circuits [Ref 1].

These four clocks can be routed to various GTX transceiver and GTH transceiver reference clock inputs through FPGA control over the I^2C interface to the crosspoint switches.

Table 1-26: **Differential SMA Connector to 8 x 8 Crosspoint Switch Clock Connections**

SMA Connector Reference Designator	Input SMA Clock Net Name	ICS85311AMLF Buffer Input Pin Number	ICS85311AMLF Buffer Output Pin Number	3.3V LVPECL Differential Clock Net Name	SN65LVCP408PAP 8 x 8 Crosspoint Switch Pin Number
J167	CLK_DIFF_0_P	U98.7	U98.1	CLK_DIFF_0_Q0_P	U57.5
J168	CLK_DIFF_0_N	U98.6	U98.2	CLK_DIFF_0_Q0_N	U57.6
			U98.3	CLK_DIFF_0_Q1_P	U58.5
			U98.4	CLK_DIFF_0_Q1_N	U58.6
J169	CLK_DIFF_1_P	U99.7	U99.1	CLK_DIFF_1_Q0_P	U57.11
J170	CLK_DIFF_1_P	U99.6	U99.2	CLK_DIFF_1_Q0_N	U57.12
			U99.3	CLK_DIFF_1_Q1_P	U58.11
			U99.4	CLK_DIFF_1_Q1_N	U58.12
J171	CLK_DIFF_2_P	U96.7	U96.1	CLK_DIFF_2_Q0_P	U57.18
J172	CLK_DIFF_2_P	U96.6	U96.2	CLK_DIFF_2_Q0_N	U57.19
			U96.3	CLK_DIFF_2_Q1_P	U58.18
			U96.4	CLK_DIFF_2_Q1_N	U58.19
J9	CLK_DIFF_3_P	U97.7	U97.1	CLK_DIFF_3_Q0_P	U57.24
J10	CLK_DIFF_3_P	U97.6	U97.2	CLK_DIFF_3_Q0_N	U57.25

Table 1-26: **Differential SMA Connector to 8 x 8 Crosspoint Switch Clock Connections *(Cont'd)***

SMA Connector Reference Designator	Input SMA Clock Net Name	ICS85311AMLF Buffer Input Pin Number	ICS85311AMLF Buffer Output Pin Number	3.3V LVPECL Differential Clock Net Name	SN65LVCP408PAP 8 x 8 Crosspoint Switch Pin Number
			U97.3	CLK_DIFF_3_Q1_P	U58.24
			U97.4	CLK_DIFF_3_Q1_N	U58.25

Differential 2.5V Si570 LVDS Oscillators

See Figure 1-2 callout [39].

The ML631 board provides four I^2C programmable Silicon Labs Si570 3.3V LVDS 10-MHz to 810-MHz oscillators. Each oscillator is connected to a 1-to-2 3.3V LVPECL ICS85311AMLF clock buffer (U43, U44, U51, and U52, respectively). The eight clock buffer outputs have net names of SI570_<CH#>_Q0 _P/N and SI570_<CH#>_Q1 _P/N, where channel number <CH#> ranges from 0 to 3. These connect to the four odd inputs (1, 3, 5, and 7) on each of the two TI SN65LVCP408PAP 8 x 8 crosspoint switch ICs U57 and U58 (nets …Q0_P/N to U57 and nets …Q1_P/N to U58). Table 1-27 traces the path of the clock pair nets from the source Si570 output pin pair to the destination crosspoint switch input pins.

Refer to the Fixed and Custom Frequencies example design files found at the link at [Ref 24] for ML631 Si570 programming details. The example design files are:

- Fixed Frequencies: `xtp122.pdf` and `rdf0144.zip`
- Custom Frequencies: `xtp121.pdf` and `rdf0143.zip`

The Si570 data sheet can be found at the Silicon Labs website [Ref 22]. Search for *Si570 programming* for the data sheet and for Silicon Labs application notes about programming the device.

Refer to *ML631 Schematic* pages 10, 11, and 14 for these circuits [Ref 1].

These four clocks can be routed to various GTX transceiver and GTH transceiver reference clock inputs through FPGA control over the I^2C interface to the crosspoint switches.

Table 1-27: **Differential Si570 to 8 x 8 Crosspoint Switch Clock Connections**

Si570 Reference Designator	Output Clock Net Name	ICS85311AMLF Buffer Input Pin Number	ICS85311AMLF Buffer Output Pin Number	3.3V LVPECL Differential Clock Net Name	SN65LVCP408PAP 8 x 8 Crosspoint Switch Pin Number
U52.4	SI570_0_P	U56.7	U56.1	SI570_0_Q0_P	U57.8
U52.5	SI570_0_N	U56.6	U56.2	SI570_0_Q0_N	U57.9
			U56.3	SI570_0_Q1_P	U58.8
			U56.4	SI570_0_Q1_N	U58.9
U51.4	SI570_1_P	U55.7	U55.1	SI570_1_Q0_P	U57.14
U51.5	SI570_1_P	U55.6	U55.2	SI570_1_Q0_N	U57.15
			U55.3	SI570_1_Q1_P	U58.14
			U55.4	SI570_1_Q1_N	U58.15

Table 1-27: **Differential Si570 to 8 x 8 Crosspoint Switch Clock Connections *(Cont'd)***

Si570 Reference Designator	Output Clock Net Name	ICS85311AMLF Buffer Input Pin Number	ICS85311AMLF Buffer Output Pin Number	3.3V LVPECL Differential Clock Net Name	SN65LVCP408PAP 8 x 8 Crosspoint Switch Pin Number
U44.4	SI570_2_P	U54.7	U54.1	SI570_2_Q0_P	U57.21
U44.5	SI570_2_P	U54.6	U54.2	SI570_2_Q0_N	U57.22
			U54.3	SI570_2_Q1_P	U58.21
			U54.4	SI570_2_Q1_N	U58.22
U43.4	SI570_3_P	U53.7	U531	SI570_3_Q0_P	U57.27
U43.5	SI570_3_P	U53.6	U53.2	SI570_3_Q0_N	U57.28
			U53.3	SI570_3_Q1_P	U58.27
			U53.4	SI570_3_Q1_N	U58.28

Differential SN65LVLVCP408PAP 8 x 8 Crosspoint Switches

See Figure 1-2 callout [40].

The ML631 board provides two I^2C programmable TI SN65LVCP408PAP 8 x 8 crosspoint switch ICs U57 and U58. Each switch has its four even inputs (0, 2, 4, and 6) connected to the differential SMA clock sources. Each switch has its four odd inputs (1, 3, 5, and 7) connected to Si570 clock sources. Refer to *ML631 Schematic* page 14 to view U57 and U58 connectivity [Ref 1]. The data sheet for the TI SN65LVCP408PAP can be found at www.ti.com [Ref 19].

U1 FPGA Differential SMA Test Clock Inputs

See Figure 1-2 callout [41, 43].

The ML631 board provides a differential input test clock SMA pair for each of the two FPGAs U1 and U2. The U1 FPGA SMA pair J124 and J125 drive the inputs of a 3.3V LVDS 1-to-6 ICS854S006AGILF differential clock buffer U126. Four of the six output pairs are used and are wired to two dual 2-to-1 ICS85356AGILF differential clock multiplexers U102 and U115. The remaining two U126 buffer output pairs are NC (no connects). Each multiplexer gets two of the four pairs as inputs. The other two multiplexer input pairs are driven from 8 x 8 crosspoint switch outputs. Each of the two multiplexer outputs can therefore be sourced from either the test clock SMA clock, or a clock from the 8 x 8 crosspoint switch, which itself has SMA clock and Si570 clock input options.

The multiplexer output pairs drive U1 GTH transceiver 106, 107, and 108 and U1 GTH transceiver 116, 117, and 118 reference clock inputs.

The U1 FPGA differential SMA test clock input connections and expansion through the 1-to-6 buffer U126 are detailed in Table 1-28. Refer to *ML631 Schematic*, page 12 for this circuit [Ref 1].

Table 1-28: **U1 FPGA SMA to Buffered Differential Test Clock Connections**

U1 FPGA Test SMA	SMA Differential Clock Net Names	ICS854S006AGILF U126 1-to-6 Buffer Output Net Names	ICS8535AGILF Dual 2-to-1 Multiplexer Input Pin Number
J124	TEST_CLK_1_P	U1_TEST_REFCLK0_P	U102.1
J125	TEST_CLK_1_N	U1_TEST_REFCLK0_N	U102.2
		U1_TEST_REFCLK1_P	U102.6
		U1_TEST_REFCLK1_N	U102.7
		U1_TEST_REFCLK2_P	U115.1
		U1_TEST_REFCLK2_N	U115.2
		U1_TEST_REFCLK3_P	U115.6
		U1_TEST_REFCLK3_N	U115.7

U2 FPGA Differential SMA Test Clock Inputs

See Figure 1-2 callout [42, 43].

Similar to the U1 FPGA test clock SMA input, the ML631 board provides a differential input test clock SMA pair for the U2 FPGA. SMA pair J126 and J127 drive the inputs of a 3.3V LVDS 1-to-6 ICS854S006AGILF differential clock buffer U127. The six output pairs created are wired to three dual 2-to-1 ICS85356AGILF differential clock multiplexers U120, U121, and U122. Each multiplexer gets two of the six pairs as inputs. The other two multiplexer input pairs are driven from 8 x 8 crosspoint switch outputs. Each of the two multiplexer outputs can therefore be sourced from either the test clock SMA clock, or a clock from the 8 x 8 crosspoint switch, which itself has SMA clock and Si570 clock input options.

The multiplexer output pairs drive U2 GTH transceiver 106, 107, and 108 and U2 GTH transceiver 116, 117, and 118 reference clock inputs.

The U2 FPGA differential SMA test clock input connections and expansion through the 1-to-6 buffer U126 are detailed in Table 1-29. Refer to *ML631 Schematic*, page 13 for this circuit [Ref 1].

Table 1-29: **U2 FPGA SMA to Buffered Differential Test Clock Connections**

U2 FPGA Test SMA	SMA Differential Clock Net Names	ICS854S006AGILF U126 1-to-6 Buffer Output Net Names	ICS8535AGILF Dual 2-to-1 Multiplexer Input Pin Number
J126	TEST_CLK_2_P	U2_TEST_REFCLK0_P	U120.1
J127	TEST_CLK_2_N	U2_TEST_REFCLK0_N	U120.2
		U2_TEST_REFCLK1_P	U120.6
		U2_TEST_REFCLK1_N	U120.7
		U2_TEST_REFCLK2_P	U121.1
		U2_TEST_REFCLK2_N	U121.2

Table 1-29: **U2 FPGA SMA to Buffered Differential Test Clock Connections *(Cont'd)***

U2 FPGA Test SMA	SMA Differential Clock Net Names	ICS854S006AGILF U126 1-to-6 Buffer Output Net Names	ICS8535AGILF Dual 2-to-1 Multiplexer Input Pin Number
		U2_TEST_REFCLK3_P	U121.6
		U2_TEST_REFCLK3_N	U121.7
		U2_TEST_REFCLK4_P	U122.1
		U2_TEST_REFCLK4_N	U122.2
		U2_TEST_REFCLK5_P	U122.6
		U2_TEST_REFCLK5_N	U122.7

U1 and U2 FPGA Si570 with 1-to-6 Clock Buffer (Two Circuits)

See Figure 1-2 callout [44].

The U1 FPGA and the U2 FPGA each have an I^2C programmable Silicon Labs Si570 3.3V LVDS 10-MHz to 810-MHz oscillator connected to a 1-to-6 ICS854S006AGILF differential clock buffer (U64–U13 and U65–U18, respectively). Refer to Differential 2.5V Si570 LVDS Oscillators, page 36, for links to further information about the Si570. The six buffer output pairs are shared between U1 and U2 as shown in Table 1-30 and Table 1-31. Refer to *ML631 Schematic* page 15 for U64, and page 69 for U65 [Ref 1].

Table 1-30: **Si570 U64 Driven Additional U1 and U2 Differential Clock Sources**

U1 FPGA Si570 U64	Si570 Differential Clock Net Names	ICS854S006AGILF 1-to-6 Buffer Output Net Names	Destination Pin Number
U64.4	SI570_4_P	U1_SI570_4_P	U1.N12
U64.5	SI570_4_N	U1_SI570_4_N	U1.M12
		U2_SI570_4_P	U2.N11
		U2_SI570_4_N	U2.M10
		U1_MGTREFCLK1_104_P	U1.Y35
		U1_MGTREFCLK1_104_N	U1.Y36
		U2_MGTREFCLK1_114_P	U2.Y10
		U2_MGTREFCLK1_114_N	U2.Y9
		U1_P1_TX_REFCLK_P	P1.A1
		U1_P1_TX_REFCLK_P	P1.B1
		U1_P2_TX_REFCLK_P	P2.A1
		U1_P2_TX_REFCLK_P	P2.B1

Table 1-31: **Si570 U65 Driven Additional U1 and U2 Differential Clock Sources**

U2 FPGA Si570 U65	Si570 Differential Clock Net Names	ICS854S006AGILF 1-to-6 Buffer Output Net Names	Destination Pin Number
U65.4	SI570_5_P	U1_SI570_5_P	U1.N11
U65.5	SI570_5_N	U1_SI570_5_N	U1.M10
		U2_SI570_5_P	U2.N12
		U2_SI570_5_N	U2.M12
		U1_MGTREFCLK1_112_P	U1.AH10
		U1_MGTREFCLK1_112_N	U1.AH9
		U2_MGTREFCLK1_1112_P	U2.AH10
		U2_MGTREFCLK1_112_N	U2.AH9
		U1_P4_TX_REFCLK_P	P4.A1
		U1_P4_TX_REFCLK_P	P4.B1

U1 and U2 FPGA GTH Transceiver Clock Routing Example

Setup of U1 and U2 GTH Transceiver Quad 106 and 107 Clocks

U1 and U2 FPGA GTH transceiver Quads 106 and 107 can be driven by Si570 oscillator U65 as follows:

- Si570 U65 is programmed to the desired frequency. The block diagram in Figure 1-7 shows the example path. Si570 U65 is connected to 1-to-6 clock driver U18, which in turn drives a TX REFCLK copy to FCI Airmax connector P4.
- To deliver the U65 Si570 frequency to U1 FPGA GTH transceiver 106 or 107, an external add-on card is required. This add-on card wraps the P4 TX REFCLK signal to J4 RX REFCLK.
- J4 RX REFCLK signals are wired to a pair of SMA connectors J134 and J135, which make the REFCLK available as a clock source.

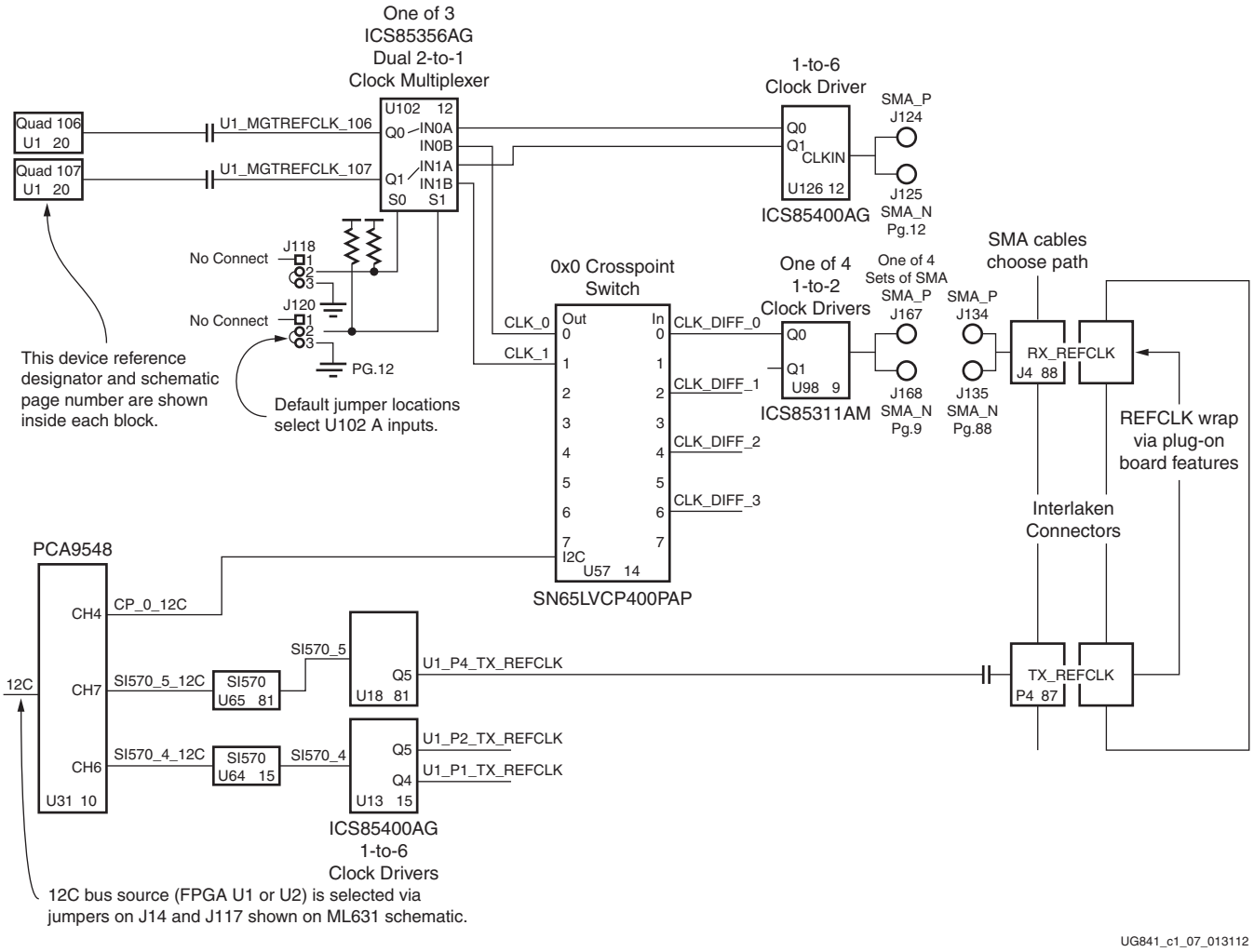

Figure 1-7: **ML631 U1 FPGA GTH Transceiver Quads 106 and 107 Clock Routing Example**

This example describes routing J4 RX REFCLK on SMA pair J134/J135 (*ML631 Schematic* page 88) to SMA pair J124/J125 (*ML631 Schematic* page 12), and J124/J125 are wired to 1-to-6 clock driver U126. Two outputs of U126 are connected to dual 2-to-1 clock multiplexer U102, which in turn is wired to U1 GTH transceiver Quads 106 and 107 [Ref 1].

Dual 2-to-1 clock multiplexer U102 has two select pins, one for each independent multiplexer. Each select pin is wired to a 3-pin header. Header J118 pin 2 is pulled up and sources the lower multiplexer (0) select signal U1_SEL0. J118 pin 1 is not connected. J118 pin 3 is wired to ground. Jumping J118 pin 3 to pin 2 forces the lower multiplexer to select its A input. When no shunt is installed on J118,its pin 2 is pulled up, which forces the lower multiplexer to select its B input.

Similarly, header J120 sources the upper multiplexer (1) select signal U1_SEL1. J120 pin 1 is not connected. J120 pin 3 is wired to ground. Jumping J120 pin 3 to pin 2 forces the upper multiplexer to select its A input. When no shunt is installed on J120, its pin 2 is pulled up, which forces the upper multiplexer to select its B input.

Table 1-32 shows the clock connection path from the J124/J125 input SMA connector clock buffer U126 to the target U1 FPGA GTH transceiver Quad 106 and 107 clock input pins.

Table 1-32: **ML631 U1 FPGA GTH Transceiver Reference Clocks**

Clock Source	Pin Number	Output	Output Clock Net Name (P/N)	Dual 2-to-1 Multiplexer			Output Pin Number	Output Clock Net Name (P/N)	Pin Number	U1 GTH Transceiver
				Input	Pin Number	Ref. Des.				
U126 1-to-6 Driver	5/6	Q0	U1_TEST_REFCLK0	CLK0A	1/2	U102	19/18	U1_MGTREFCLK_106_C_P/N	R41	106
U57 Crosspoint Switch	60/59	0	CLK_0	CLK0B	4/5	U102			R42	
U126 1-to-6 Driver	8/9	Q1	U1_TEST_REFCLK1	CLK1A	6/7	U102	13/12	U1_MGTREFCLK_107_C_P/N	J41	107
U57 Crosspoint Switch	57/56	1	CLK_1	CLK1B	9/10	U102			J42	
U126 1-to-6 Driver	11/12	Q2	U1_TEST_REFCLK2	CLK0A	1/2	U115	19/18	U1_MGTREFCLK_108_C_P/N	E41	108
U57 Crosspoint Switch	54/53	2	CLK_2	CLK0B	4/5	U115			E42	

Note: All GTH transceiver REFCLK inputs are AC-coupled.

U2 FPGA Quads 106 and 107 can similarly be driven from the J4 RX REFCLK, as shown in Figure 1-8.

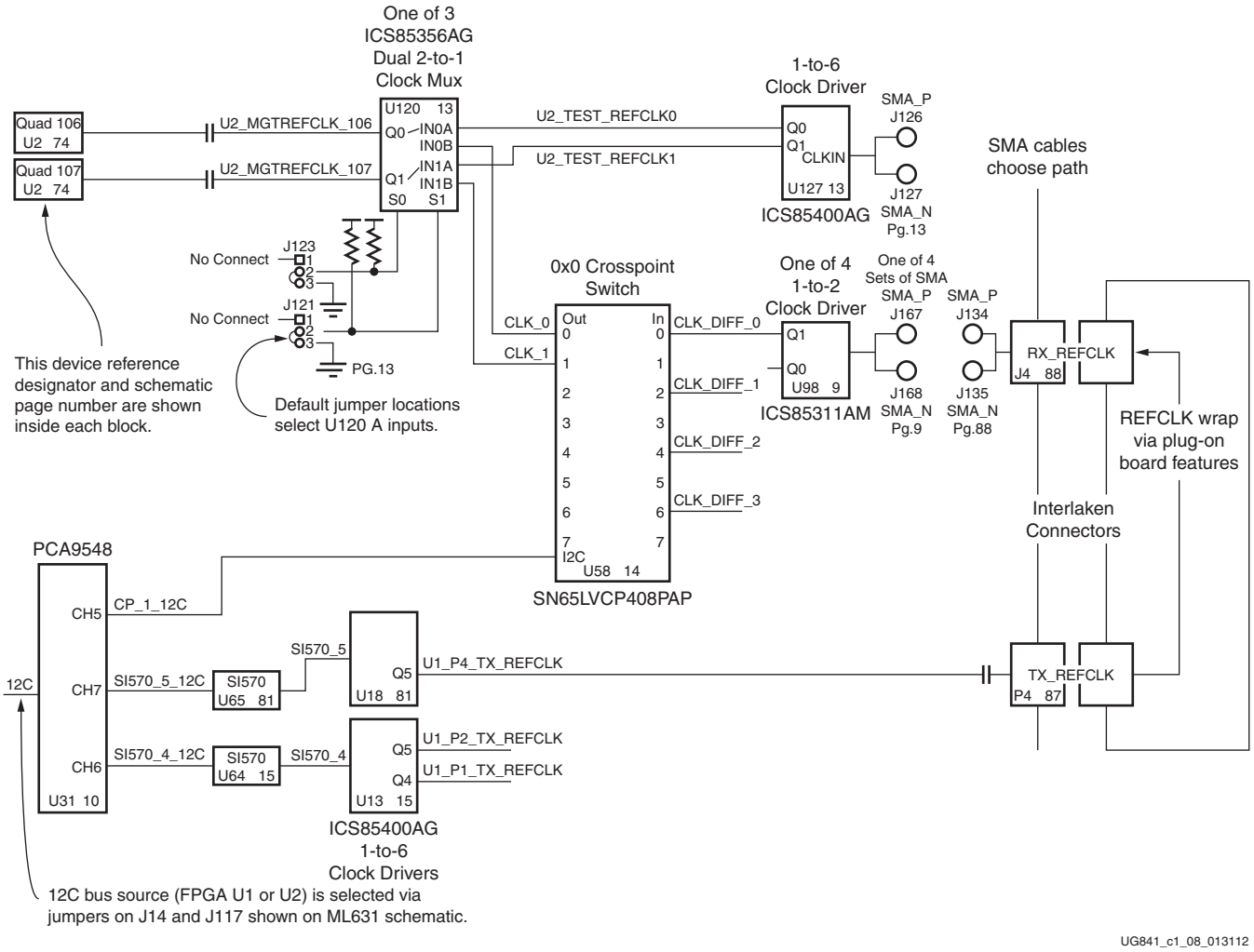

Figure 1-8: **ML631 U2 FPGA GTH Transceiver Quads 106 and 107 U2 GTH Transceiver Clock Routing Diagram**

This second example (Figure 1-8 and Table 1-33) describes routing J4 RX REFCLK on SMA pair J134/J135 to SMA pair J126/J127. J126/J127 are wired to 1-to-6 clock driver U127. Two outputs of U127 are connected to dual 2-to-1 clock multiplexer U120, which in turn is wired to U2 GTH transceiver Quads 106 and 107.

Dual 2-to-1 clock multiplexer U120 has two select pins, one for each independent multiplexer. Each select pin is wired to a 3-pin header. Header J123 pin 2 is pulled up and sources the lower multiplexer (0) select signal U2_SEL0. J123 pin 1 is not connected. J123 pin 3 is wired to ground. Jumping J123 pin 3 to pin 2 forces the lower multiplexer to select its A input. When no shunt is installed on J123, its pin 2 is pulled up, which forces the lower multiplexer to select its B input.

Similarly, header J121 sources the upper multiplexer (1) select signal U2_SEL1. J121 pin 1 is not connected. J121 pin 3 is wired to ground. Jumping J121 pin 3 to pin 2 forces the upper multiplexer to select its A input. When no shunt is installed on J121, its pin 2 is pulled up, which forces the upper multiplexer to select its B input.

Table 1-33 shows the clock connection path from the J126/J127 input SMA connector clock buffer U127 to the target U2 FPGA GTH transceiver Quad 106 and 107 clock input pins.

Table 1-33: **ML631 U2 FPGA GTH Transceiver Reference Clocks**

Clock Source	Pin Number	Output	Output Clock Net Name (P/N)	Dual 2-to-1 Multiplexer			Output Pin Number	Output Clock Net Name (P/N)	Pin Number	U2 GTH
				Input	Pin Number	Ref. Des.				
U127 1-to-6 Driver	5/6	Q0	U2_TEST_REFCLK0	CLK0A	1/2	U120	19/18	U2_MGTREFCLK_106_C_P/N	R41	106
U58 Crosspoint Switch	60/59	0	CLK_8	CLK0B	4/5	U120			R42	
U127 1-to-6 Driver	8/9	Q1	U2_TEST_REFCLK1	CLK1A	6/7	U120	13/12	U2_MGTREFCLK_107_C_P/N	J41	107
U58 Crosspoint Switch	57/56	1	CLK_9	CLK1B	9/10	U120			J42	
U127 1-to-6 Driver	11/12	Q2	U2_TEST_REFCLK2	CLK0A	1/2	U121	19/18	U2_MGTREFCLK_108_C_P/N	E41	108
U58 Crosspoint Switch	54/53	2	CLK_10	CLK0B	4/5	U121			E42	
U127 1-to-6 Driver	13/14	Q3	U2_TEST_REFCLK3	CLK1A	6/7	U121	13/12	U2_MGTREFCLK_118_C_P/N	E4	118
U58 Crosspoint Switch	51/50	3	CLK_11	CLK1B	9/10	U121			E3	
U127 1-to-6 Driver	16/17	Q4	U2_TEST_REFCLK4	CLK0A	1/2	U122	19/18	U2_MGTREFCLK_116_C_P/N	R4	116
U58 Crosspoint Switch	43/42	4	CLK_12	CLK0B	4/5	U122			R3	
U127 1-to-6 Driver	19/20	Q5	U2_TEST_REFCLK5	CLK1A	6/7	U122	13/12	U2_MGTREFCLK_117_C_P/N	J4	117
U58 Crosspoint Switch	40/39	5	CLK_13	CLK1B	9/10	U122			J3	

Note: Dual 2-to-1 multiplexer “B” input clk_n clock nets are sourced from 8 x 8 crosspoint switch U58. All GTH transceiver REFCLK inputs are AC-coupled.

System Monitor

See Figure 1-2 callout [1, 2].

The U1 and U2 FPGA System Monitor bank 0 AVDD and AVSS power pins are tied to filtered FPGA V_{CCAUX} (see *ML631 Schematic* pages 17 and 83 for U1 and U2, respectively) to allow internal use of the System Monitor functions [Ref 1]. The external System Monitor pins are used for general purpose I/O.

I2C Bus Management

See Figure 1-2 callout [45].

The ML631 main I2C bus can be sourced from either the U1 or U2 FPGA. Each FPGA has a I2C_SCL/SDA_MAIN bus connected to bus selection 3-pin headers J14 and J117, shown on *ML631 Schematic* page 10 [Ref 1]. The headers allow selection of either the U1 or U2 I2C bus as the I2C active bus. The header is wired to a level-shifter IC (U128), so the selected low voltage 1.5V FPGA bus is translated to 3.3V for interfacing to the bus residents. I2C bus topology is shown in Figure 1-9.

There are two bus targets on the main 3.3V I2C bus:

- I2C EEPROM M24C02 256x8 U59 address 50 or 54
- I2C 1-to-8 bus switch PCS9548 U31 address 70 or 74

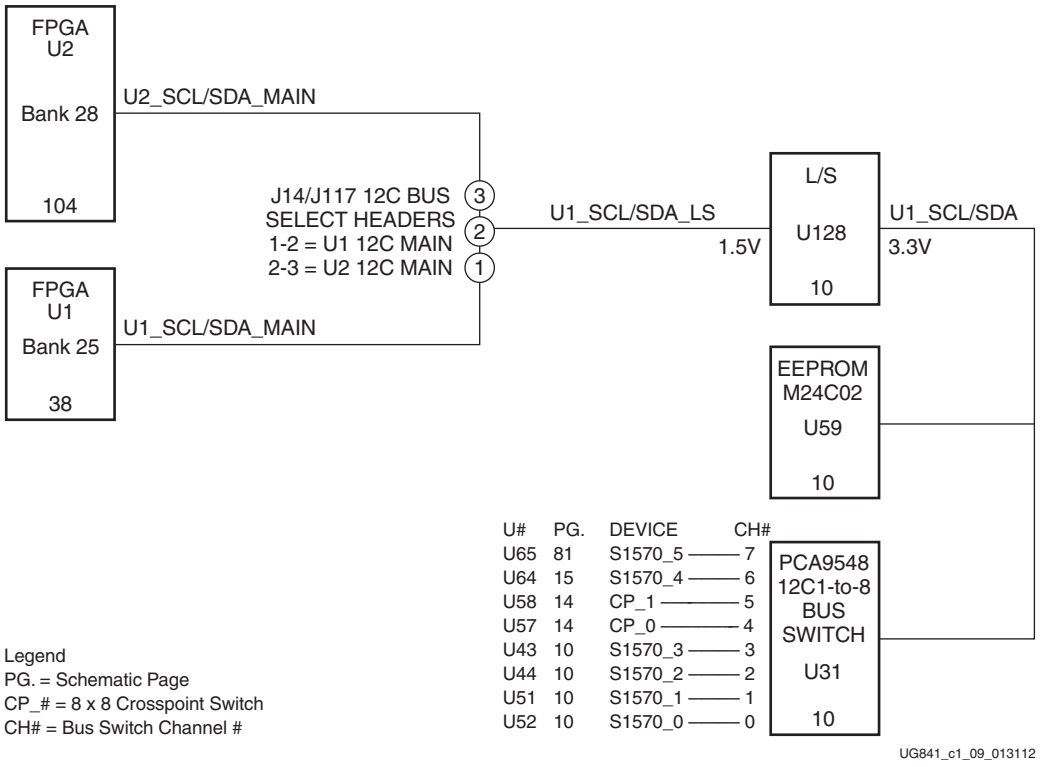

Figure 1-9: **I2C Bus Connection Diagram**

Notes relevant to Figure 1-9:

- L/S = TI TXS0104 level-shifter device. The number at the bottom of each box is the *ML631 Schematic* page number for that component [Ref 1].
- *ML631 Schematic* page 10 shows 3-pin headers J21, J18, and J100, that can be used to change the I2C address of U59 and U31.
- U59 EEPROM I2C ADDR = `0x50` or `0x54`.
- U31 I2C bus switch I2C ADDR = `0x70` or `0x74`.

The pin connections of the I2C bus components are detailed in Table 1-34.

Table 1-34: **I²C Bus Connections: U1 and U2 FPGA Main I²C Bus**

FPGA Pin Number	I²C Bus Net Name	I²C Bus Headers	I²C Bus Headers	I²C Bus Net Name	L/S U128 1.5V	L/S U128 3.3V	I²C Bus Net Name	PCA9548 U31	M24C02 EEPROM U59
U1.N32	U1_SCL_MAIN	J14.1							
U1.P31	U1_SDA_MAIN	J117.1	J14.2	U1_SCL_LS	U128.2	U128.13	U1_SCL	U31.22	U59.6
U2.J25	U2_SCL_MAIN	J14.3	J117.2	U1_SDA_LS	U128.3	U128.12	U1_SDA	U31.23	U59.5
U2.K25	U2_SDA_MAIN	J117.3							

An I²C component on the back side of the I²C switch can be accessed by selecting the appropriate channel through the control register of the PCS9548 I²C bus switch U31 as shown in Table 1-35.

Table 1-35: **I²C Bus Switch Channel Assignments**

U31 Channel (1)	I²C Component
0	Si570_0 I²C programmable clock U52 address 5D
1	Si570_1 I²C programmable clock U51 address 5D
2	Si570_2 I²C programmable clock U44 address 5D
3	Si570_3 I²C programmable clock U43 address 5D
4	CP_0 8 x 8 Crosspoint Switch U57 address 2C
5	CP_1 8 x 8 Crosspoint Switch U58 address 2C
6	Si570_4 I²C programmable clock U64 address 5D
7	Si570_5 I²C programmable clock U65 address 5D

Notes:

1. Refer to the *ML631 Schematic*, page 10 [Ref 1]. U31 I2C ADDR = `0x70` with E2 = 0 and `0x74` with E2=1

FCI Airmax Plug and Receptacle Level-Shifted Control Signals

See Figure 1-2 callouts [31, 32, 33].

FCI Airmax plug (P1, P2, and P4) and receptacle (J1, J2, and J4) connectors each support a group of three 3.3V control signals requiring level shifting. The three signals on each of the six connectors are called CK, DATA, and SYNC. The connections are detailed in Table 1-36. The level shifters for P1/J1, P2/J2, and P4/J4 are on *ML631 Schematic*, pages 27, 24, and 88, respectively [Ref 1].

Table 1-36: **ML631 Airmax Connector Level-Shifted Control Signals**

FCI Connector Reference Designator	Net Name (3.3V Side)	TXB0104DR Level Shifter Pin Number	Net Name (2.5V Side)	U1 FPGA Pin Number
P1		U104		
P1.E10	U1_AMH1_FC_CK	U104.13	U1_AMH1_FC_LS_CK	U1.A10
P1.H7	U1_AMH1_FC_DATA	U104.12	U1_AMH1_FC_LS_DATA	U1.B11

Table 1-36: **ML631 Airmax Connector Level-Shifted Control Signals *(Cont'd)***

FCI Connector Reference Designator	Net Name (3.3V Side)	TXB0104DR Level Shifter Pin Number	Net Name (2.5V Side)	U1 FPGA Pin Number
P1.H9	U1_AMH1_FC_SYNC	U104.11	U1_AMH1_FC_LS_SYNC	U1.A12
J1		U103		
J1.E10	U1_AMR1_FC_CK	U103.13	U1_AMR1_FC_LS_CK	U1.A13
J1.H7	U1_AMR1_FC_DATA	U103.12	U1_AMR1_FC_LS_DATA	U1.C11
J1.H9	U1_AMR1_FC_SYNC	U103.11	U1_AMR1_FC_LS_SYNC	U1.C12
P2		U105		
P1.E10	U1_AMH2_FC_CK	U105.13	U1_AMH2_FC_LS_CK	U1.B12
P1.H7	U1_AMH2_FC_DATA	U105.12	U1_AMH2_FC_LS_DATA	U1.C13
P1.H9	U1_AMH2_FC_SYNC	U105.11	U1_AMH2_FC_LS_SYNC	U1.A8
J2		U106		
J1.E10	U1_AMR2_FC_CK	U106.13	U1_AMR2_FC_LS_CK	U1.B9
J1.H7	U1_AMR2_FC_DATA	U106.12	U1_AMR2_FC_LS_DATA	U1.R12
J1.H9	U1_AMR2_FC_SYNC	U106.11	U1_AMR2_FC_LS_SYNC	U1.R13
P4		U109		
P1.E10	U2_AMH4_FC_CK	U109.13	U2_AMH4_FC_LS_CK	U2.A10
P1.H7	U2_AMH4_FC_DATA	U109.12	U2_AMH4_FC_LS_DATA	U2.B11
P1.H9	U2_AMH4_FC_SYNC	U109.11	U2_AMH4_FC_LS_SYNC	U2.A12
J4		U110		
J1.E10	U2_AMR4_FC_CK	U110.13	U2_AMR4_FC_LS_CK	U2.A13
J1.H7	U2_AMR4_FC_DATA	U110.12	U2_AMR4_FC_LS_DATA	U2.C11
J1.H9	U2_AMR4_FC_SYNC	U110.11	U2_AMR4_FC_LS_SYNC	U2.C12

U1 Memory Configuration

See Figure 1-2 callout [46].

U1 FPGA DDR3 Component Memory

The U1 FPGA supports nine DDR3 32-bit memory interfaces, each of which require a memory controller implementation in the FPGA interconnect logic. See the block diagram in Figure 1-10.

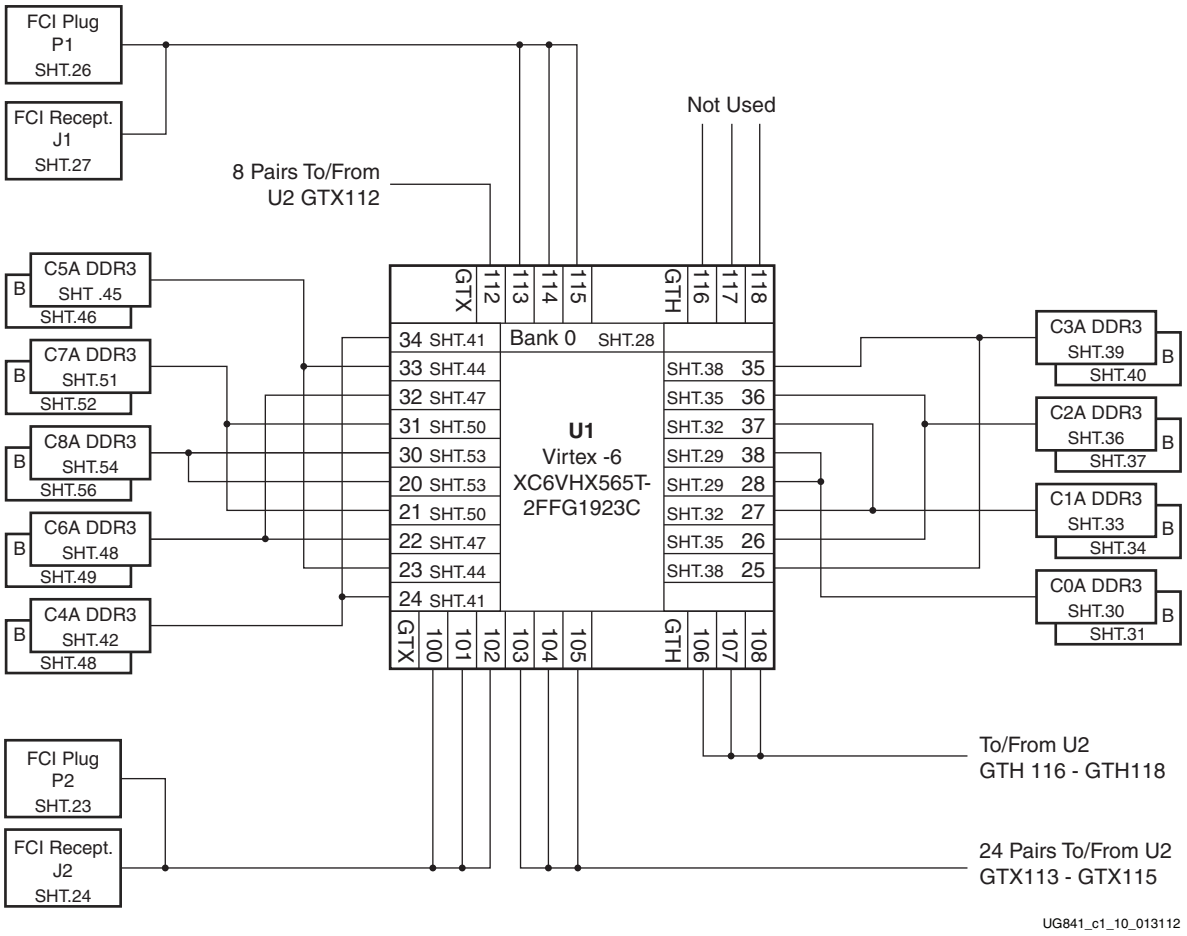

Figure 1-10: **U1 FPGA 32-Bit Data Path DDR3 Memory Block Diagram**

Each pair of Micron MT41J128M16HA-15 128 Mb x 16 memories provides a 512 MB block of memory to the U1 FPGA. All the U1 FPGA DDR3 memory controller interfaces must use internal V_{REF} and DCI cascade. U1 banks 27 and 37 are the DCI masters.

U2 Memory Configuration

See Figure 1-2 callout [47].

U2 FPGA Component Memory

The U2 FPGA has three types of memory components attached:

- The U2 FPGA supports four Micron MT41J128M16HA-15 128 Mb x 16 (256 MB) DDR3 memory interfaces, each of which require a memory controller implementation in the FPGA interconnect logic.
- The U2 FPGA also supports two Cypress CY7C1565KV18-400BZXC 2 Mb x 36 (9 MB) QDRII+ memory interfaces, each of which require a memory controller implementation in the FPGA interconnect logic.
- Finally, the U2 FPGA also supports two Cypress CY7C12481KV18-400BZXC 2 Mb x 18 (4.5 MB) DDR2 SRAM memory interfaces, each of which require a memory controller implementation in the FPGA interconnect logic.

See the block diagram in Figure 1-11.

This memory component combination provides a total memory size of 1046.5 MB available to the U2 FPGA. All memory controller interfaces must use internal VREF and DCI cascade. FPGA U2 Banks 22 and 32 are the DCI masters.

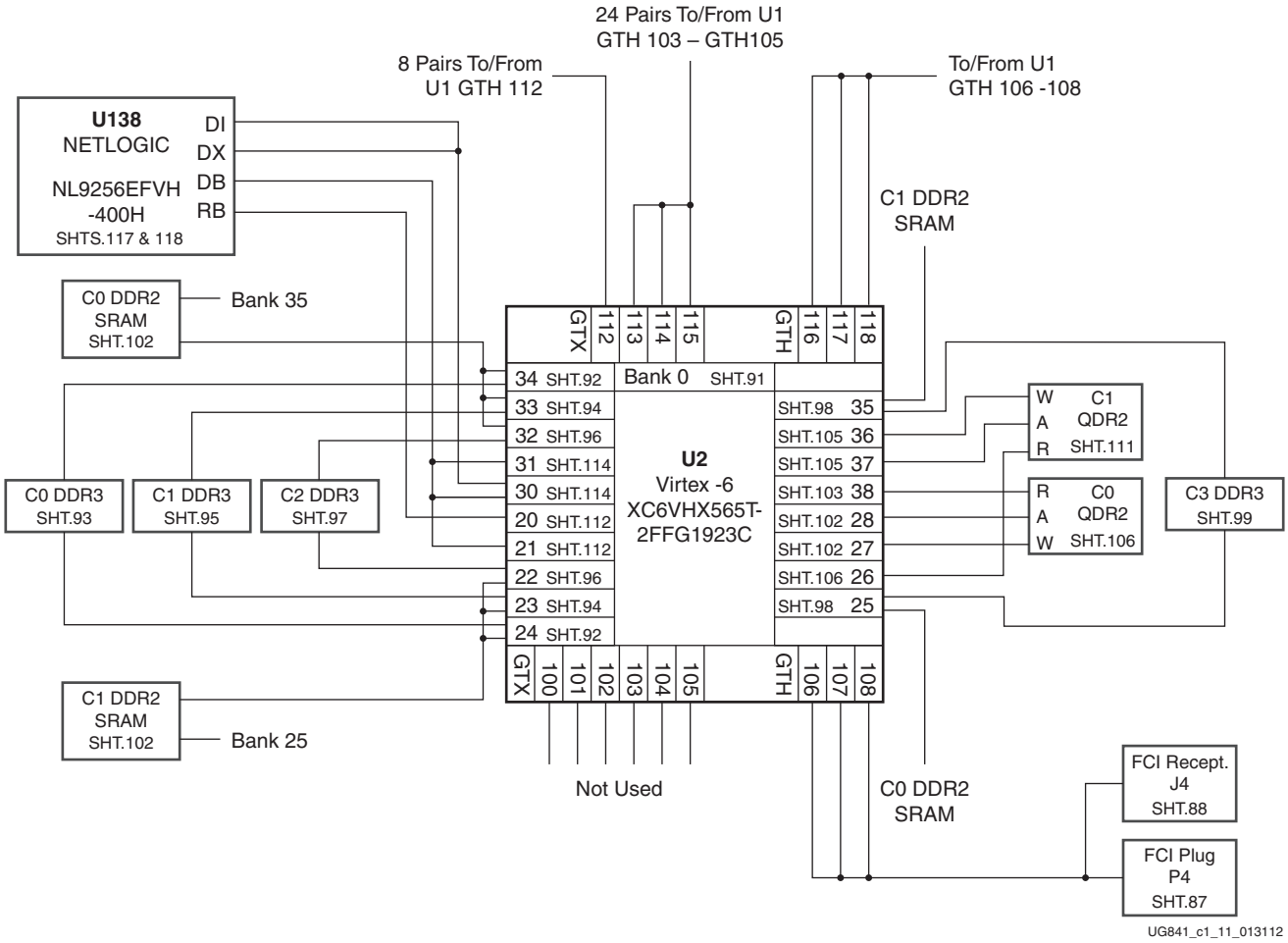

Figure 1-11: **U2 FPGA Memory Block Diagram**

NetLogic Microsystems NL92000 Series Network Processor Adjunct on the U2 FPGA

See Figure 1-2 callout [48].

The ML631 hosts a NL9256EFVH-400H knowledge-based processor.

The NetLogic Microsystems processor interface is connected to U2 banks 20, 21, 30, and 31. See Figure 1-11, which shows the processor connections. Figure 1-11 also shows NetLogic Microsystems processor U138 in the upper left corner.

More information about the NetLogic Microsystems NL9256 can be found at the NetLogic Microsystems website [Ref 25].

U2 FPGA VGA Debug Connector

The U2 FPGA supports a 2x5 VGA debug header J60. The debug header provides three color signals (RGB) along with VSYNC and HSYNC. Each of the color signals is generated by the summation of four FPGA pin outputs driven through stepped resistor values. To see the implementation for the U2 FPGA debug connector J60, refer to *ML631 Schematic* [Ref 1], pages 104 (FPGA U2 connections), page 119 (scaling resistors and debug header J60), and Table 1-37.

Table 1-37: **U2 FPGA VGA Debug J60**

U2 FPGA Pin Number	Net Name	Scaling Resistor	Net Name	J60 Debug Connector Pin Number
J23	U1_VGA_VSYNC	R1072	U2_VSYNC	2
H23	U1_VGA_HSYNC	R1071	U2_HSYNC	4
H26	U1_VGA_B_0	R993	U2_BLUE	6
J26	U1_VGA_B_1	R1263		
N24	U1_VGA_B_2	R1034		
N23	U1_VGA_B_3	R1031		
F25	U1_VGA_G_0	R992	U2_GREEN	8
G24	U1_VGA_G_1	R1078		
H24	U1_VGA_G_2	R1033		
J24	U1_VGA_G_3	R1026		
P24	U1_VGA_R_0	R991	U2_RED	10
P23	U1_VGA_R_1	R1077		
G26	U1_VGA_R_2	R1032		
G25	U1_VGA_R_3	R1025		

Appendix A

Default Shunt Positions

Table A-1 lists the standard (black) shunts that must be installed on the board for proper operation. Refer to the *ML631 Schematic* [Ref 1].

Table A-1: **Default Shunt Positions**

Shunts on Headers	Description	ML631 Schematic Page
J65-1 to J65-2	Enable System ACE red error LED	5
J14-1 to J14-2	Set U1 SCL as IIC bus master	10
J117-1 to J117-2	Set U1 SDA as IIC bus master	10
J21-2 to J21-3	Set GA0 to 0 (GND)	10
J18-2 to J18-3	Set GA1 to 0 (GND)	10
J100-1 to J100-2	Set EEPROM E2 address to 0 (GND)	10
J118-2 to J118-3	U1_GTHREFCLK = SMA J124/J125	12
J120-2 to J120-3	U1_GTHREFCLK = SMA J124/J125	12
J123-2 to J123-3	U2_GTHREFCLK = SMA J126/J127	13
J121-2 to J121-3	U2_GTHREFCLK = SMA J126/J127	13
J136-2 to J136-3	Enable the U1 FPGA in JTAG chain	28
J22-2 to J22-3	Enable ON/OFF switch to turn on UCD9240 controllers	65
J289 no shunt	Inhibit all UCD9240 controlled power supplies from operating. This shunt is installed ***only*** for CM programming of the UCD9240 power supplies.	66
J137-2 to J137-3	Enable FPGA U2 in JTAG chain	91
J101-1 to J101-2	U139 DDRII+ SRAM ENABLE PLL (DDRII+ mode)	100
J103-2 to J103-3	U139 DDRII+ SRAM ODT = 0 (GND) (ODT not supported on device)	100
J107-1 to J107-2	U140 DDRII+ SRAM ENABLE PLL (DDRII+ mode)	102
J104-2 to J104-3	U140 DDRII+ SRAM ODT = 0 (GND) (ODT not supported on device)	102
J16-2 to J16-3	U136 QDRII+ SRAM ZQ = 250Ω	106
J23-1 to J23-2	U136 QDRII+ SRAM ENABLE PLL = QDRII+ mode	106

Table A-1: **Default Shunt Positions *(Cont'd)***

Shunts on Headers	Description	ML631 Schematic Page
J24-2 to J24-3	U137 QDRII+ SRAM ZQ = 250Ω	111
J46-1 to J46-2	U137 QDRII+ SRAM ENABLE PLL = QDRII+ mode	111
J47-2 to J47-3	NL_FSEL0 = 0 (Low), select = 250 to 400 MHz	117
J58-1 to J58-2	NL_FSEL1 = 1 (High), select = 250 to 400 MHz	117
J48-1 to J48-2	NL_SREN mode select	117
J87-1 to J87-2	NL_HSIM mode select	117
J109-2 to J109-3	NL_TIM = 0 HSIM selects interface mode (NL9K)	117
J110-1 to J110-2	NL_ODAMOD mode select. Output data edge-aligned	117

Appendix B

ML631 Master UCF Listing for U1

The ML631 master user constraints file (UCF) template provides for designs targeting the ML631 Virtex-6 HXT FPGA Packet Processor/Traffic Manager evaluation board. Net names in the constraints listed in this appendix correlate with net names on the *ML631 Schematic* [Ref 1]. Users must identify the appropriate pins and replace the net names in this appendix with net names in the user RTL. See UG625, *Constraints Guide*, for more information [Ref 3].

```
##################################################################
##
##  ML631 REV C PIN LISTING: INITIAL RELEASE
##
##  FPGA U1: HX565T-2FFG1923C
##  Note: 1 additional CCIO "P" NC pin in 2X banks (Rev C)
##
##  Note: Memory designs must use internal VREF for any bank
##        with SSTL15 inputs.
##        Example: CONFIG INTERNAL_VREF_BANK34=0.75;
##
##  Note:
##
##   BANK 37 is DCI MASTER for DDR3 DCI CASCADE in column 3X
##   BANK 27 is DCI MASTER for DDR3 DCI CASCADE in column 2X
##
##################################################################
#
# NET  VRN_37          LOC =  J18; # Bank  37
# NET  VRP_37          LOC =  N18; # Bank  37
# NET  VRN_27          LOC =  R26; # Bank  27
# NET  VRP_27          LOC =  P26; # Bank  27
##################################################################


#####################################
####
####  FPGA U1 IIC INTERFACE
####  IOSTANDARD = LVCMOS15
####  3.3V LEVEL SHIFTERS ON PCB
####
#####################################

 NET  U1_SDA_MAIN    LOC =  P31; # Bank  25
 NET  U1_SCL_MAIN    LOC =  N32; # Bank  25

#####################################
##
```

```
##  FPGA U1 GLOBAL CLOCK INPUTS
##  USE IOSTANDARD = DIFF_SSTL15
##  100 OHM TERMINATION ON PCB
##
#######################################

 NET  CLK200_P        LOC =  R31; # Bank  25
 NET  CLK200_N        LOC =  R32; # Bank  25
 NET  SI570_4_P       LOC =  J33; # Bank  25
 NET  SI570_4_N       LOC =  H33; # Bank  25
 NET  SI570_5_P       LOC =  N12; # Bank  35
 NET  SI570_5_N       LOC =  M12; # Bank  35

#######################################
##
##  FPGA U1 8x8 CROSSPOINT CLOCK CONTROLS
##  IOSTANDARD = LVCMOS15
##
##  NOTE:
##  RESET MUST BE ASSERTED & DEASSERTED
##  BY FPGA TO AVOID POTENTIAL POWER UP
##  TRISTATE CLOCK OUTPUT SITUATION
##  RESET GUARANTEES OUTPUTS ENABLED
##
#######################################

 NET  CP_1_RES_B      LOC =  T27; # Bank  27
 NET  CP_1_SWT        LOC =  R27; # Bank  27
 NET  CP_0_RES_B      LOC =  J28; # Bank  27
 NET  CP_0_SWT        LOC =  J29; # Bank  27

###########################################
##
##  User Pushbuttons : logic 1 when pressed
##  IOSTANDARD = LVCMOS15
##
###########################################

 NET  U1_USER_PB4     LOC = AR18; # Bank  30
 NET  U1_USER_PB3     LOC =  J25; # Bank  28 (AV17 on Rev B)
 NET  U1_USER_PB2     LOC =  H26; # Bank  28 (H11 on Rev B)
 NET  U1_USER_PB1     LOC =  H34; # Bank  25

#####################################
##
##  USER LEDS IOSTANDARD = LVCMOS15
##
#####################################

 NET  U1_USER_LED4   LOC =  K22; # Bank  38
 NET  U1_USER_LED3   LOC =  D21; # Bank  38
 NET  U1_USER_LED2   LOC =  N23; # Bank  38 (M21 on Rev B)
 NET  U1_USER_LED1   LOC =  K25; # Bank  28

#####################################
##
##  CHIP-TO-CHIP I/O
##  U1 to U2 all 1.5V banks
##
```

```
#####################################
NET  U1_U2_C2CIO0    LOC =  BC31;
NET  U1_U2_C2CIO1    LOC =  BB31;
NET  U1_U2_C2CIO2    LOC =  AM29;
NET  U1_U2_C2CIO3    LOC =  AL29;
NET  U1_U2_C2CIO4    LOC =  AY30;
NET  U1_U2_C2CIO5    LOC =  AM32;
NET  U1_U2_C2CIO6    LOC =  AM31;
NET  U1_U2_C2CIO7    LOC =  N24;
NET  U1_U2_C2CIO8    LOC =  AK16;
NET  U1_U2_C2CIO9    LOC =  AL14;
NET  U1_U2_C2CIO10   LOC =  BD28;
NET  U1_U2_C2CIO11   LOC =  BC28;
NET  U1_U2_C2CIO12   LOC =  AK25;
NET  U1_U2_C2CIO13   LOC =  AJ24;
NET  U1_U2_C2CIO14   LOC =  BA24;
NET  U1_U2_C2CIO15   LOC =  AK26;
NET  U1_U2_C2CIO16   LOC =  AJ25;
NET  U1_U2_C2CIO17   LOC =  BA12;
NET  U1_U2_C2CIO18   LOC =  J26;
NET  U1_U2_C2CIO19   LOC =  BA10;
NET  U1_U2_C2CIO20   LOC =  F25;

#####################################
##
## INTERLAKEN Flow Control Signals
##  and general purpose I/O signals
##  1.5V to 3.3V level shifters on PCB
##
#####################################

## P1 flow control signals
NET  U1_AMH1_FC_LS_CK     LOC = BD33;
NET  U1_AMH1_FC_LS_DATA   LOC = BC33;
NET  U1_AMH1_FC_LS_SYNC   LOC = AL33;

## J1 flow control signals
NET  U1_AMR1_FC_LS_CK     LOC = AK32;
NET  U1_AMR1_FC_LS_DATA   LOC = BA34;
NET  U1_AMR1_FC_LS_SYNC   LOC = AL34;

## P1 I/O controls:

NET  U1_AMH1_LS_IO0       LOC = BB24;
NET  U1_AMH1_LS_IO1       LOC = BA24;
NET  U1_AMH1_LS_IO2       LOC = AP24;
NET  U1_AMH1_LS_IO3       LOC = AN24;
NET  U1_AMH1_LS_IO4       LOC = AU24;
NET  U1_AMH1_LS_IO5       LOC = AR25;
NET  U1_AMH1_LS_IO6       LOC = AP25;
NET  U1_AMH1_LS_IO7       LOC = AJ18;


## P2 flow control signals
NET  U1_AMH2_FC_LS_CK     LOC = J30;
NET  U1_AMH2_FC_LS_DATA   LOC = K30;
NET  U1_AMH2_FC_LS_SYNC   LOC = T30;

## J2 flow control signals
```

```
NET  U1_AMR2_FC_LS_CK     LOC = T29;
NET  U1_AMR2_FC_LS_DATA   LOC = G32;
NET  U1_AMR2_FC_LS_SYNC   LOC = M32;

## P2 I/O controls:

NET  U1_AMH2_LS_IO0       LOC = AV21;
NET  U1_AMH2_LS_IO1       LOC = AU21;
NET  U1_AMH2_LS_IO2       LOC = AN22;
NET  U1_AMH2_LS_IO3       LOC = AN23;
NET  U1_AMH2_LS_IO4       LOC = AY21;
NET  U1_AMH2_LS_IO5       LOC = AU20;
NET  U1_AMH2_LS_IO6       LOC = AT20;
NET  U1_AMH2_LS_IO7       LOC = AP21;

############################
## MIG MEMORY INTERFACES:
############################


##########################################
##
##  32-bit DDR3 Controller C8
##
##########################################

NET  U1_C8_DDR3_CLK_P          LOC = BC18; # Bank  30
NET  U1_C8_DDR3_CLK_N          LOC = BD18; # Bank  30

NET  U1_C8_DDR3_CKE            LOC = BC14; # Bank  30
NET  U1_C8_DDR3_CS_B           LOC = BA18; # Bank  30

NET  U1_C8_DDR3_A13            LOC = BC16; # Bank  30
NET  U1_C8_DDR3_A12            LOC = BB15; # Bank  30
NET  U1_C8_DDR3_A11            LOC = BD13; # Bank  30
NET  U1_C8_DDR3_A10            LOC = BD15; # Bank  30
NET  U1_C8_DDR3_A9             LOC = BD16; # Bank  30
NET  U1_C8_DDR3_A8             LOC = BD11; # Bank  30
NET  U1_C8_DDR3_A7             LOC = AY16; # Bank  30
NET  U1_C8_DDR3_A6             LOC = BB14; # Bank  30
NET  U1_C8_DDR3_A5             LOC = AY17; # Bank  30
NET  U1_C8_DDR3_A4             LOC = BD10; # Bank  30
NET  U1_C8_DDR3_A3             LOC = AW16; # Bank  30
NET  U1_C8_DDR3_A2             LOC = BC17; # Bank  30
NET  U1_C8_DDR3_A1             LOC = BD14; # Bank  30
NET  U1_C8_DDR3_A0             LOC = AV16; # Bank  30

NET  U1_C8_DDR3_BA0            LOC = BC13; # Bank  30
NET  U1_C8_DDR3_BA1            LOC = BC12; # Bank  30
NET  U1_C8_DDR3_BA2            LOC = BB16; # Bank  30

NET  U1_C8_DDR3_RAS_B          LOC = BC11; # Bank  30
NET  U1_C8_DDR3_CAS_B          LOC = AV17; # Bank  30 (AT17 on Rev B)
NET  U1_C8_DDR3_WE_B           LOC = AU16; # Bank  30
NET  U1_C8_DDR3_ODT            LOC = AR20; # Bank  30
NET  U1_C8_DDR3_RESET_B        LOC = AY18; # Bank  30
##
##  Byte lane 0
##
```

```
NET  U1_C8_DDR3_DQS0_P          LOC = BB21; # Bank  20
NET  U1_C8_DDR3_DQS0_N          LOC = BC21; # Bank  20
NET  U1_C8_DDR3_DQ0             LOC = BD23; # Bank  20
NET  U1_C8_DDR3_DQ1             LOC = BC19; # Bank  20
NET  U1_C8_DDR3_DQ2             LOC = BC23; # Bank  20
NET  U1_C8_DDR3_DQ3             LOC = BD19; # Bank  20
NET  U1_C8_DDR3_DQ4             LOC = BD21; # Bank  20
NET  U1_C8_DDR3_DQ5             LOC = AT22; # Bank  20
NET  U1_C8_DDR3_DQ6             LOC = BD20; # Bank  20
NET  U1_C8_DDR3_DQ7             LOC = AT23; # Bank  20
##
##  Byte lane 1
##
NET  U1_C8_DDR3_DQS1_P          LOC = AU22; # Bank  20
NET  U1_C8_DDR3_DQS1_N          LOC = AV22; # Bank  20
NET  U1_C8_DDR3_DQ8             LOC = BA19; # Bank  20
NET  U1_C8_DDR3_DQ9             LOC = BC22; # Bank  20
NET  U1_C8_DDR3_DQ10            LOC = AV19; # Bank  20
NET  U1_C8_DDR3_DQ11            LOC = BB22; # Bank  20
NET  U1_C8_DDR3_DQ12            LOC = AW19; # Bank  20
NET  U1_C8_DDR3_DQ13            LOC = BB19; # Bank  20
NET  U1_C8_DDR3_DQ14            LOC = AR21; # Bank  20
NET  U1_C8_DDR3_DQ15            LOC = BA22; # Bank  20
##
##  Byte lane 2
##
NET  U1_C8_DDR3_DQS2_P          LOC = AP23; # Bank  20
NET  U1_C8_DDR3_DQS2_N          LOC = AR23; # Bank  20
NET  U1_C8_DDR3_DQ16            LOC = AW20; # Bank  20
NET  U1_C8_DDR3_DQ17            LOC = AY20; # Bank  20
NET  U1_C8_DDR3_DQ18            LOC = AW21; # Bank  20
NET  U1_C8_DDR3_DQ19            LOC = AY23; # Bank  20
NET  U1_C8_DDR3_DQ20            LOC = AW23; # Bank  20
NET  U1_C8_DDR3_DQ21            LOC = BB20; # Bank  20
NET  U1_C8_DDR3_DQ22            LOC = AV23; # Bank  20
NET  U1_C8_DDR3_DQ23            LOC = BA23; # Bank  20
##
##  Byte lane 3
##
NET  U1_C8_DDR3_DQS3_P          LOC = AP20; # Bank  30
NET  U1_C8_DDR3_DQS3_N          LOC = AP19; # Bank  30
NET  U1_C8_DDR3_DQ24            LOC = AW18; # Bank  30
NET  U1_C8_DDR3_DQ25            LOC = AU17; # Bank  30
NET  U1_C8_DDR3_DQ26            LOC = BA17; # Bank  30
NET  U1_C8_DDR3_DQ27            LOC = AU19; # Bank  30
NET  U1_C8_DDR3_DQ28            LOC = AV18; # Bank  30
NET  U1_C8_DDR3_DQ29            LOC = AT18; # Bank  30
NET  U1_C8_DDR3_DQ30            LOC = BB17; # Bank  30
NET  U1_C8_DDR3_DQ31            LOC = AT19; # Bank  30
##
## MIG Reserved CCIO "P" NC Pins
##
#NET  No Connect                 LOC = AR22; # Bank  20 MRCC
#NET  No Connect                 LOC = AY22; # Bank  20 MRCC
#NET  No Connect                 LOC = BA20; # Bank  20 SRCC
#NET  No Connect                 LOC = BB12; # Bank  30 SRCC
#NET  No Connect                 LOC = AT17; # Bank  30 MRCC (Rev C)

##############################################
```

```
##
##  32-bit DDR3 Controller C7
##
##########################################

NET  U1_C7_DDR3_CLK_P          LOC = AY15; # Bank  31
NET  U1_C7_DDR3_CLK_N          LOC = BA15; # Bank  31

NET  U1_C7_DDR3_CKE            LOC = AN21; # Bank  31
NET  U1_C7_DDR3_CS_B           LOC = AR17; # Bank  31

NET  U1_C7_DDR3_A13            LOC = AV14; # Bank  31
NET  U1_C7_DDR3_A12            LOC = BA14; # Bank  31
NET  U1_C7_DDR3_A11            LOC = BA13; # Bank  31
NET  U1_C7_DDR3_A10            LOC = AM21; # Bank  31
NET  U1_C7_DDR3_A9             LOC = AW15; # Bank  31
NET  U1_C7_DDR3_A8             LOC = AY13; # Bank  31
NET  U1_C7_DDR3_A7             LOC = AU14; # Bank  31
NET  U1_C7_DDR3_A6             LOC = AW13; # Bank  31
NET  U1_C7_DDR3_A5             LOC = AK20; # Bank  31
NET  U1_C7_DDR3_A4             LOC = AV13; # Bank  31
NET  U1_C7_DDR3_A3             LOC = AL20; # Bank  31
NET  U1_C7_DDR3_A2             LOC = AL19; # Bank  31
NET  U1_C7_DDR3_A1             LOC = AW14; # Bank  31
NET  U1_C7_DDR3_A0             LOC = AM20; # Bank  31

NET  U1_C7_DDR3_BA0            LOC = AR16; # Bank  31 (AT14 on Rev B)
NET  U1_C7_DDR3_BA1            LOC = AT13; # Bank  31
NET  U1_C7_DDR3_BA2            LOC = AU15; # Bank  31

NET  U1_C7_DDR3_RAS_B          LOC = AT15; # Bank  31
NET  U1_C7_DDR3_CAS_B          LOC = AJ20; # Bank  31
NET  U1_C7_DDR3_WE_B           LOC = AJ19; # Bank  31
NET  U1_C7_DDR3_ODT            LOC = AK18; # Bank  31
NET  U1_C7_DDR3_RESET_B        LOC = AP18; # Bank  31
##
##  Byte lane 0
##
NET  U1_C7_DDR3_DQS0_P         LOC = AW26; # Bank  21
NET  U1_C7_DDR3_DQS0_N         LOC = AY26; # Bank  21
NET  U1_C7_DDR3_DQ0            LOC = AT25; # Bank  21
NET  U1_C7_DDR3_DQ1            LOC = AK23; # Bank  21
NET  U1_C7_DDR3_DQ2            LOC = AU25; # Bank  21
NET  U1_C7_DDR3_DQ3            LOC = AJ23; # Bank  21
NET  U1_C7_DDR3_DQ4            LOC = BA25; # Bank  21
NET  U1_C7_DDR3_DQ5            LOC = AM26; # Bank  21
NET  U1_C7_DDR3_DQ6            LOC = BB25; # Bank  21
NET  U1_C7_DDR3_DQ7            LOC = AN26; # Bank  21
##
##  Byte lane 1
##
NET  U1_C7_DDR3_DQS1_P         LOC = AK22; # Bank  21
NET  U1_C7_DDR3_DQS1_N         LOC = AL23; # Bank  21
NET  U1_C7_DDR3_DQ8            LOC = AY25; # Bank  21
NET  U1_C7_DDR3_DQ9            LOC = AV26; # Bank  21
NET  U1_C7_DDR3_DQ10           LOC = AW24; # Bank  21
NET  U1_C7_DDR3_DQ11           LOC = AU26; # Bank  21
NET  U1_C7_DDR3_DQ12           LOC = AW25; # Bank  21
NET  U1_C7_DDR3_DQ13           LOC = AR26; # Bank  21
```

```
NET  U1_C7_DDR3_DQ14           LOC = AM22; # Bank  21
NET  U1_C7_DDR3_DQ15           LOC = AP26; # Bank  21
##
##  Byte lane 2
##
NET  U1_C7_DDR3_DQS2_P         LOC = AL24; # Bank  21
NET  U1_C7_DDR3_DQS2_N         LOC = AM24; # Bank  21
NET  U1_C7_DDR3_DQ16           LOC = BC24; # Bank  21
NET  U1_C7_DDR3_DQ17           LOC = AM25; # Bank  21
NET  U1_C7_DDR3_DQ18           LOC = BD24; # Bank  21
NET  U1_C7_DDR3_DQ19           LOC = BC26; # Bank  21
NET  U1_C7_DDR3_DQ20           LOC = AL25; # Bank  21
NET  U1_C7_DDR3_DQ21           LOC = BD26; # Bank  21
NET  U1_C7_DDR3_DQ22           LOC = AT24; # Bank  21
NET  U1_C7_DDR3_DQ23           LOC = BD25; # Bank  21
##
##  Byte lane 3
##
NET  U1_C7_DDR3_DQS3_P         LOC = AJ21; # Bank  31
NET  U1_C7_DDR3_DQS3_N         LOC = AK21; # Bank  31
NET  U1_C7_DDR3_DQ24           LOC = AM17; # Bank  31
NET  U1_C7_DDR3_DQ25           LOC = AP15; # Bank  31
NET  U1_C7_DDR3_DQ26           LOC = AL18; # Bank  31
NET  U1_C7_DDR3_DQ27           LOC = AP16; # Bank  31
NET  U1_C7_DDR3_DQ28           LOC = AM19; # Bank  31
NET  U1_C7_DDR3_DQ29           LOC = AN18; # Bank  31
NET  U1_C7_DDR3_DQ30           LOC = AN17; # Bank  31
NET  U1_C7_DDR3_DQ31           LOC = AN19; # Bank  31
##
## MIG Reserved CCIO "P" NC Pins
##
#NET  No Connect               LOC = AL22; # Bank  21 MRCC
#NET  No Connect               LOC = AV24; # Bank  21 MRCC
#NET  No Connect               LOC = BB26; # Bank  21 SRCC
#NET  No Connect               LOC = AT14; # Bank  31 MRCC (Rev C)
#NET  No Connect               LOC = AR15; # Bank  31 SRCC

##########################################
##
##  32-bit DDR3 Controller C6
##
##########################################

NET  U1_C6_DDR3_CLK_P          LOC =  AW1; # Bank  32
NET  U1_C6_DDR3_CLK_N          LOC =  AY1; # Bank  32

NET  U1_C6_DDR3_CKE            LOC =  BD4; # Bank  32
NET  U1_C6_DDR3_CS_B           LOC =  AY5; # Bank  32

NET  U1_C6_DDR3_A13            LOC =  BC4; # Bank  32
NET  U1_C6_DDR3_A12            LOC =  BD3; # Bank  32
NET  U1_C6_DDR3_A11            LOC =  BA2; # Bank  32
NET  U1_C6_DDR3_A10            LOC =  BC3; # Bank  32
NET  U1_C6_DDR3_A9             LOC =  BA3; # Bank  32
NET  U1_C6_DDR3_A8             LOC =  AY2; # Bank  32
NET  U1_C6_DDR3_A7             LOC =  BD5; # Bank  32
NET  U1_C6_DDR3_A6             LOC =  BB1; # Bank  32
NET  U1_C6_DDR3_A5             LOC =  BA4; # Bank  32
NET  U1_C6_DDR3_A4             LOC =  BC2; # Bank  32
```

```
NET  U1_C6_DDR3_A3              LOC =  AY3; # Bank  32
NET  U1_C6_DDR3_A2              LOC =  BD8; # Bank  32
NET  U1_C6_DDR3_A1              LOC =  BB2; # Bank  32
NET  U1_C6_DDR3_A0              LOC =  BD9; # Bank  32

NET  U1_C6_DDR3_BA0             LOC =  BC8; # Bank  32
NET  U1_C6_DDR3_BA1             LOC =  BC7; # Bank  32
NET  U1_C6_DDR3_BA2             LOC =  BA5; # Bank  32

NET  U1_C6_DDR3_RAS_B           LOC =  BB4; # Bank  32
NET  U1_C6_DDR3_CAS_B           LOC =  AW5; # Bank  32 (BC6 on Rev B)
NET  U1_C6_DDR3_WE_B            LOC =  BD6; # Bank  32
NET  U1_C6_DDR3_ODT             LOC = BB11; # Bank  32
NET  U1_C6_DDR3_RESET_B         LOC =  BB6; # Bank  32 (AW5 on Rev B)
##
##  Byte lane 0
##
NET  U1_C6_DDR3_DQS0_P          LOC = AV29; # Bank  22
NET  U1_C6_DDR3_DQS0_N          LOC = AW29; # Bank  22
NET  U1_C6_DDR3_DQ0             LOC = AP29; # Bank  22
NET  U1_C6_DDR3_DQ1             LOC = AK28; # Bank  22
NET  U1_C6_DDR3_DQ2             LOC = AP28; # Bank  22
NET  U1_C6_DDR3_DQ3             LOC = AJ28; # Bank  22
NET  U1_C6_DDR3_DQ4             LOC = AT28; # Bank  22
NET  U1_C6_DDR3_DQ5             LOC = AN29; # Bank  22
NET  U1_C6_DDR3_DQ6             LOC = AR28; # Bank  22
NET  U1_C6_DDR3_DQ7             LOC = AN28; # Bank  22
##
##  Byte lane 1
##
NET  U1_C6_DDR3_DQS1_P          LOC = AL27; # Bank  22
NET  U1_C6_DDR3_DQS1_N          LOC = AL28; # Bank  22
NET  U1_C6_DDR3_DQ8             LOC = AK27; # Bank  22
NET  U1_C6_DDR3_DQ9             LOC = AV27; # Bank  22
NET  U1_C6_DDR3_DQ10            LOC = AR27; # Bank  22
NET  U1_C6_DDR3_DQ11            LOC = AT27; # Bank  22
NET  U1_C6_DDR3_DQ12            LOC = AU29; # Bank  22
NET  U1_C6_DDR3_DQ13            LOC = BA28; # Bank  22
NET  U1_C6_DDR3_DQ14            LOC = AT29; # Bank  22
NET  U1_C6_DDR3_DQ15            LOC = AY28; # Bank  22
##
##  Byte lane 2
##
NET  U1_C6_DDR3_DQS2_P          LOC = AM27; # Bank  22
NET  U1_C6_DDR3_DQS2_N          LOC = AN27; # Bank  22
NET  U1_C6_DDR3_DQ16            LOC = BA29; # Bank  22
NET  U1_C6_DDR3_DQ17            LOC = BD29; # Bank  22
NET  U1_C6_DDR3_DQ18            LOC = AY27; # Bank  22
NET  U1_C6_DDR3_DQ19            LOC = BC29; # Bank  22
NET  U1_C6_DDR3_DQ20            LOC = BB27; # Bank  22
NET  U1_C6_DDR3_DQ21            LOC = BB29; # Bank  22
NET  U1_C6_DDR3_DQ22            LOC = AW28; # Bank  22
NET  U1_C6_DDR3_DQ23            LOC = BC27; # Bank  22
##
##  Byte lane 3
##
NET  U1_C6_DDR3_DQS3_P          LOC = BB10; # Bank  32
NET  U1_C6_DDR3_DQS3_N          LOC =  BC9; # Bank  32
NET  U1_C6_DDR3_DQ24            LOC = AY10; # Bank  32
```

```
NET  U1_C6_DDR3_DQ25           LOC =  BB9; # Bank  32
NET  U1_C6_DDR3_DQ26           LOC =  BA7; # Bank  32
NET  U1_C6_DDR3_DQ27           LOC =  BA9; # Bank  32
NET  U1_C6_DDR3_DQ28           LOC =  BB7; # Bank  32
NET  U1_C6_DDR3_DQ29           LOC = AY11; # Bank  32
NET  U1_C6_DDR3_DQ30           LOC =  BA8; # Bank  32
NET  U1_C6_DDR3_DQ31           LOC = AY12; # Bank  32
##
## MIG Reserved NC Pins
##
NET  No Connect                LOC = AJ26; # Bank  22 MRCC
NET  No Connect                LOC = AU27; # Bank  22 MRCC
NET  No Connect                LOC = AV28; # Bank  22 SRCC
NET  No Connect                LOC =  BB5; # Bank  32 SRCC
NET  No Connect                LOC =  BC6; # Bank  32 MRCC (Rev C)


##########################################
##
##  32-bit DDR3 Controller C5
##
##########################################

NET  U1_C5_DDR3_CLK_P          LOC = AT12; # Bank  33
NET  U1_C5_DDR3_CLK_N          LOC = AU12; # Bank  33

NET  U1_C5_DDR3_CKE            LOC = AW11; # Bank  33
NET  U1_C5_DDR3_CS_B           LOC = AR11; # Bank  33

NET  U1_C5_DDR3_A13            LOC = AV12; # Bank  33
NET  U1_C5_DDR3_A12            LOC = AP14; # Bank  33
NET  U1_C5_DDR3_A11            LOC =  AU7; # Bank  33
NET  U1_C5_DDR3_A10            LOC = AL17; # Bank  33
NET  U1_C5_DDR3_A9             LOC =  AV6; # Bank  33
NET  U1_C5_DDR3_A8             LOC = AU10; # Bank  33
NET  U1_C5_DDR3_A7             LOC =  AW8; # Bank  33
NET  U1_C5_DDR3_A6             LOC = AW10; # Bank  33
NET  U1_C5_DDR3_A5             LOC =  AY7; # Bank  33
NET  U1_C5_DDR3_A4             LOC = AR13; # Bank  33
NET  U1_C5_DDR3_A3             LOC =  AY8; # Bank  33
NET  U1_C5_DDR3_A2             LOC =  AY6; # Bank  33
NET  U1_C5_DDR3_A1             LOC = AV11; # Bank  33
NET  U1_C5_DDR3_A0             LOC =  AW9; # Bank  33

NET  U1_C5_DDR3_BA0            LOC = AU11; # Bank  33
NET  U1_C5_DDR3_BA1            LOC = AM16; # Bank  33
NET  U1_C5_DDR3_BA2            LOC =  AV9; # Bank  33

NET  U1_C5_DDR3_ODT            LOC = AN14; # Bank  33
NET  U1_C5_DDR3_RESET_B        LOC = AP11; # Bank  33
NET  U1_C5_DDR3_RAS_B          LOC =  AW6; # Bank  33
NET  U1_C5_DDR3_CAS_B          LOC = AM15; # Bank  33 (AP13 on Rev B)
NET  U1_C5_DDR3_WE_B           LOC = AR12; # Bank  33
##
##  Byte lane 0
##
NET  U1_C5_DDR3_DQS0_P         LOC = AU32; # Bank  23
NET  U1_C5_DDR3_DQS0_N         LOC = AV32; # Bank  23
NET  U1_C5_DDR3_DQ0            LOC = AU30; # Bank  23
```

```
NET  U1_C5_DDR3_DQ1             LOC = AN31; # Bank  23
NET  U1_C5_DDR3_DQ2             LOC = AT30; # Bank  23
NET  U1_C5_DDR3_DQ3             LOC = AN32; # Bank  23
NET  U1_C5_DDR3_DQ4             LOC = AP31; # Bank  23
NET  U1_C5_DDR3_DQ5             LOC = AJ30; # Bank  23
NET  U1_C5_DDR3_DQ6             LOC = AR32; # Bank  23
NET  U1_C5_DDR3_DQ7             LOC = AJ31; # Bank  23
##
##  Byte lane 1
##
NET  U1_C5_DDR3_DQS1_P          LOC = AK31; # Bank  23
NET  U1_C5_DDR3_DQS1_N          LOC = AL32; # Bank  23
NET  U1_C5_DDR3_DQ8             LOC = AP30; # Bank  23
NET  U1_C5_DDR3_DQ9             LOC = AY31; # Bank  23
NET  U1_C5_DDR3_DQ10            LOC = AR31; # Bank  23
NET  U1_C5_DDR3_DQ11            LOC = BB30; # Bank  23
NET  U1_C5_DDR3_DQ12            LOC = AK30; # Bank  23
NET  U1_C5_DDR3_DQ13            LOC = AW31; # Bank  23
NET  U1_C5_DDR3_DQ14            LOC = AT32; # Bank  23
NET  U1_C5_DDR3_DQ15            LOC = AR30; # Bank  23
##
##  Byte lane 2
##
NET  U1_C5_DDR3_DQS2_P          LOC = AL30; # Bank  23
NET  U1_C5_DDR3_DQS2_N          LOC = AM30; # Bank  23
NET  U1_C5_DDR3_DQ16            LOC = AV31; # Bank  23
NET  U1_C5_DDR3_DQ17            LOC = BD31; # Bank  23
NET  U1_C5_DDR3_DQ18            LOC = AW30; # Bank  23
NET  U1_C5_DDR3_DQ19            LOC = BC32; # Bank  23
NET  U1_C5_DDR3_DQ20            LOC = BA32; # Bank  23
NET  U1_C5_DDR3_DQ21            LOC = BD30; # Bank  23
NET  U1_C5_DDR3_DQ22            LOC = AY32; # Bank  23
NET  U1_C5_DDR3_DQ23            LOC = BB32; # Bank  23
##
##  Byte lane 3
##
NET  U1_C5_DDR3_DQS3_P          LOC = AJ16; # Bank  33
NET  U1_C5_DDR3_DQS3_N          LOC = AJ15; # Bank  33
NET  U1_C5_DDR3_DQ24            LOC = AK17; # Bank  33
NET  U1_C5_DDR3_DQ25            LOC =  AU9; # Bank  33
NET  U1_C5_DDR3_DQ26            LOC =  AV8; # Bank  33
NET  U1_C5_DDR3_DQ27            LOC = AK15; # Bank  33
NET  U1_C5_DDR3_DQ28            LOC = AN13; # Bank  33
NET  U1_C5_DDR3_DQ29            LOC = AN12; # Bank  33
NET  U1_C5_DDR3_DQ30            LOC = AM14; # Bank  33
NET  U1_C5_DDR3_DQ31            LOC = AL15; # Bank  33
##
## MIG Reserved CCIO "P" NC Pins
##
NET  No Connect                 LOC = AJ29; # Bank  23 MRCC
NET  No Connect                 LOC = BA30; # Bank  23 SRCC
NET  No Connect                 LOC = AU31; # Bank  23 SRCC
NET  No Connect                 LOC =  AV7; # Bank  33 SRCC
NET  No Connect                 LOC = AP13; # Bank  33 MRCC (Rev C)



##############################################
##
```

```
##  32-bit DDR3 Controller C4
##
##########################################

NET  U1_C4_DDR3_CLK_P          LOC = AR10; # Bank  34
NET  U1_C4_DDR3_CLK_N          LOC = AT10; # Bank  34

NET  U1_C4_DDR3_CKE            LOC =  AV3; # Bank  34
NET  U1_C4_DDR3_CS_B           LOC =  AT8; # Bank  34

NET  U1_C4_DDR3_A13            LOC =  AU4; # Bank  34
NET  U1_C4_DDR3_A12            LOC =  AT2; # Bank  34
NET  U1_C4_DDR3_A11            LOC =  AT5; # Bank  34
NET  U1_C4_DDR3_A10            LOC =  AW4; # Bank  34
NET  U1_C4_DDR3_A9             LOC =  AW3; # Bank  34
NET  U1_C4_DDR3_A8             LOC =  AU5; # Bank  34
NET  U1_C4_DDR3_A7             LOC =  AU2; # Bank  34
NET  U1_C4_DDR3_A6             LOC =  AR5; # Bank  34
NET  U1_C4_DDR3_A5             LOC =  AU1; # Bank  34
NET  U1_C4_DDR3_A4             LOC =  AT4; # Bank  34
NET  U1_C4_DDR3_A3             LOC =  AV4; # Bank  34
NET  U1_C4_DDR3_A2             LOC =  AV2; # Bank  34
NET  U1_C4_DDR3_A1             LOC =  AT3; # Bank  34
NET  U1_C4_DDR3_A0             LOC =  AV1; # Bank  34

NET  U1_C4_DDR3_BA0            LOC = AK10; # Bank  34 (AR8 on Rev B)
NET  U1_C4_DDR3_BA1            LOC =  AT7; # Bank  34
NET  U1_C4_DDR3_BA2            LOC =  AU6; # Bank  34

NET  U1_C4_DDR3_RAS_B          LOC = AP10; # Bank  34
NET  U1_C4_DDR3_CAS_B          LOC =  AR7; # Bank  34
NET  U1_C4_DDR3_WE_B           LOC =  AR6; # Bank  34
NET  U1_C4_DDR3_ODT            LOC = AJ13; # Bank  34
NET  U1_C4_DDR3_RESET_B        LOC =  AT9; # Bank  34
##
##  Byte lane 0
##
NET  U1_C4_DDR3_DQS0_P         LOC = AP35; # Bank  24
NET  U1_C4_DDR3_DQS0_N         LOC = AR35; # Bank  24
NET  U1_C4_DDR3_DQ0            LOC = AH32; # Bank  24
NET  U1_C4_DDR3_DQ1            LOC = AT35; # Bank  24
NET  U1_C4_DDR3_DQ2            LOC = AN33; # Bank  24
NET  U1_C4_DDR3_DQ3            LOC = AH33; # Bank  24
NET  U1_C4_DDR3_DQ4            LOC = AP34; # Bank  24
NET  U1_C4_DDR3_DQ5            LOC = AR33; # Bank  24
NET  U1_C4_DDR3_DQ6            LOC = AP33; # Bank  24
NET  U1_C4_DDR3_DQ7            LOC = AU35; # Bank  24
##
##  Byte lane 1
##
NET  U1_C4_DDR3_DQS1_P         LOC = AJ33; # Bank  24
NET  U1_C4_DDR3_DQS1_N         LOC = AK33; # Bank  24
NET  U1_C4_DDR3_DQ8            LOC = AU34; # Bank  24
NET  U1_C4_DDR3_DQ9            LOC = AT33; # Bank  24
NET  U1_C4_DDR3_DQ10           LOC = AV34; # Bank  24
NET  U1_C4_DDR3_DQ11           LOC = AY33; # Bank  24
NET  U1_C4_DDR3_DQ12           LOC = AL35; # Bank  24
NET  U1_C4_DDR3_DQ13           LOC = AV33; # Bank  24
NET  U1_C4_DDR3_DQ14           LOC = AT34; # Bank  24
```

```
NET  U1_C4_DDR3_DQ15           LOC = AW34; # Bank  24
##
##  Byte lane 2
##
NET  U1_C4_DDR3_DQS2_P         LOC = AM34; # Bank  24
NET  U1_C4_DDR3_DQS2_N         LOC = AN34; # Bank  24
NET  U1_C4_DDR3_DQ16           LOC = BB34; # Bank  24
NET  U1_C4_DDR3_DQ17           LOC = BB35; # Bank  24
NET  U1_C4_DDR3_DQ18           LOC = BA35; # Bank  24
NET  U1_C4_DDR3_DQ19           LOC = BD35; # Bank  24
NET  U1_C4_DDR3_DQ20           LOC = AY35; # Bank  24
NET  U1_C4_DDR3_DQ21           LOC = BD34; # Bank  24
NET  U1_C4_DDR3_DQ22           LOC = BA33; # Bank  24
NET  U1_C4_DDR3_DQ23           LOC = BC34; # Bank  24
##
##  Byte lane 3
##
NET  U1_C4_DDR3_DQS3_P         LOC = AH13; # Bank  34
NET  U1_C4_DDR3_DQS3_N         LOC = AH12; # Bank  34
NET  U1_C4_DDR3_DQ24           LOC = AM10; # Bank  34
NET  U1_C4_DDR3_DQ25           LOC = AL13; # Bank  34
NET  U1_C4_DDR3_DQ26           LOC = AM12; # Bank  34
NET  U1_C4_DDR3_DQ27           LOC = AK12; # Bank  34
NET  U1_C4_DDR3_DQ28           LOC = AL12; # Bank  34
NET  U1_C4_DDR3_DQ29           LOC = AL10; # Bank  34
NET  U1_C4_DDR3_DQ30           LOC = AM11; # Bank  34
NET  U1_C4_DDR3_DQ31           LOC = AK11; # Bank  34
##
## MIG Reserved CCIO "P" NC Pins
##
NET  No Connect                LOC = AK35; # Bank  24 SRCC
NET  No Connect                LOC = AW33; # Bank  24 MRCC
NET  No Connect                LOC = AW35; # Bank  24 MRCC
NET  No Connect                LOC = AN11; # Bank  34 SRCC
NET  No Connect                LOC =  AR8; # Bank  34 MRCC (Rev C)


##########################################
##
##  32-bit DDR3 Controller C3
##
##########################################


NET  U1_C3_DDR3_CLK_P          LOC =  N11; # Bank  35
NET  U1_C3_DDR3_CLK_N          LOC =  M10; # Bank  35

NET  U1_C3_DDR3_CKE            LOC =  A10; # Bank  35
NET  U1_C3_DDR3_CS_B           LOC =   A9; # Bank  35

NET  U1_C3_DDR3_A13            LOC =  L10; # Bank  35
NET  U1_C3_DDR3_A12            LOC =  H12; # Bank  35
NET  U1_C3_DDR3_A11            LOC =  C12; # Bank  35
NET  U1_C3_DDR3_A10            LOC =  K12; # Bank  35
NET  U1_C3_DDR3_A9             LOC =  L12; # Bank  35
NET  U1_C3_DDR3_A8             LOC =  E11; # Bank  35
NET  U1_C3_DDR3_A7             LOC =  M11; # Bank  35
NET  U1_C3_DDR3_A6             LOC =  F10; # Bank  35
```

```
NET  U1_C3_DDR3_A5              LOC =  P10; # Bank  35
NET  U1_C3_DDR3_A4              LOC =  G11; # Bank  35
NET  U1_C3_DDR3_A3              LOC =  P11; # Bank  35
NET  U1_C3_DDR3_A2              LOC =  D10; # Bank  35
NET  U1_C3_DDR3_A1              LOC =  E10; # Bank  35
NET  U1_C3_DDR3_A0              LOC =  J10; # Bank  35

NET  U1_C3_DDR3_BA0             LOC =  H11; # Bank  35 (G12 on Rev B)
NET  U1_C3_DDR3_BA1             LOC =  F12; # Bank  35
NET  U1_C3_DDR3_BA2             LOC =  K10; # Bank  35

NET  U1_C3_DDR3_ODT             LOC =  G10; # Bank  35
NET  U1_C3_DDR3_RESET_B         LOC =  B10; # Bank  35
NET  U1_C3_DDR3_RAS_B           LOC =  D11; # Bank  35
NET  U1_C3_DDR3_CAS_B           LOC =  K11; # Bank  35
NET  U1_C3_DDR3_WE_B            LOC =  J11; # Bank  35
##
##  Byte lane 0
##
NET  U1_C3_DDR3_DQS0_P          LOC =  B37; # Bank  25
NET  U1_C3_DDR3_DQS0_N          LOC =  A37; # Bank  25
NET  U1_C3_DDR3_DQ0             LOC =  K33; # Bank  25
NET  U1_C3_DDR3_DQ1             LOC =  B35; # Bank  25
NET  U1_C3_DDR3_DQ2             LOC =  L33; # Bank  25
NET  U1_C3_DDR3_DQ3             LOC =  B36; # Bank  25
NET  U1_C3_DDR3_DQ4             LOC =  P35; # Bank  25
NET  U1_C3_DDR3_DQ5             LOC =  A35; # Bank  25
NET  U1_C3_DDR3_DQ6             LOC =  P34; # Bank  25
NET  U1_C3_DDR3_DQ7             LOC =  A34; # Bank  25
##
##  Byte lane 1
##
NET  U1_C3_DDR3_DQS1_P          LOC =  K35; # Bank  25
NET  U1_C3_DDR3_DQS1_N          LOC =  J35; # Bank  25
NET  U1_C3_DDR3_DQ8             LOC =  C34; # Bank  25
NET  U1_C3_DDR3_DQ9             LOC =  B34; # Bank  25
NET  U1_C3_DDR3_DQ10            LOC =  D34; # Bank  25
NET  U1_C3_DDR3_DQ11            LOC =  D33; # Bank  25
NET  U1_C3_DDR3_DQ12            LOC =  E35; # Bank  25
NET  U1_C3_DDR3_DQ13            LOC =  N34; # Bank  25
NET  U1_C3_DDR3_DQ14            LOC =  D35; # Bank  25
NET  U1_C3_DDR3_DQ15            LOC =  L35; # Bank  25
##
##  Byte lane 2
##
NET  U1_C3_DDR3_DQS2_P          LOC =  R33; # Bank  25
NET  U1_C3_DDR3_DQS2_N          LOC =  P33; # Bank  25
NET  U1_C3_DDR3_DQ16            LOC =  E33; # Bank  25
NET  U1_C3_DDR3_DQ17            LOC =  M34; # Bank  25
NET  U1_C3_DDR3_DQ18            LOC =  F33; # Bank  25
NET  U1_C3_DDR3_DQ19            LOC =  L34; # Bank  25
NET  U1_C3_DDR3_DQ20            LOC =  F35; # Bank  25
NET  U1_C3_DDR3_DQ21            LOC =  G34; # Bank  25
NET  U1_C3_DDR3_DQ22            LOC =  F34; # Bank  25
NET  U1_C3_DDR3_DQ23            LOC =  J34; # Bank  25
##
##  Byte lane 3
##
NET  U1_C3_DDR3_DQS3_P          LOC =  R13; # Bank  35
```

```
NET  U1_C3_DDR3_DQS3_N          LOC =  R12; # Bank  35
NET  U1_C3_DDR3_DQ24            LOC =  A13; # Bank  35
NET  U1_C3_DDR3_DQ25            LOC =   B9; # Bank  35
NET  U1_C3_DDR3_DQ26            LOC =  B12; # Bank  35
NET  U1_C3_DDR3_DQ27            LOC =   A8; # Bank  35
NET  U1_C3_DDR3_DQ28            LOC =  C13; # Bank  35
NET  U1_C3_DDR3_DQ29            LOC =  A12; # Bank  35
NET  U1_C3_DDR3_DQ30            LOC =  C11; # Bank  35
NET  U1_C3_DDR3_DQ31            LOC =  B11; # Bank  35
##
## MIG Reserved CCIO "P" NC Pins
##
#NET  No Connect                 LOC =  N33; # Bank  25 MRCC
#NET  No Connect                 LOC =  M35; # Bank  25 MRCC
#NET  No Connect                 LOC =  G35; # Bank  25 SRCC
#NET  No Connect                 LOC =  E12; # Bank  35 SRCC
#NET  No Connect                 LOC =  G12; # Bank  35 MRCC (Rev C)


##########################################
##
##  32-bit DDR3 Controller C2
##
##########################################

NET  U1_C2_DDR3_CLK_P           LOC =  K15; # Bank  36
NET  U1_C2_DDR3_CLK_N           LOC =  J15; # Bank  36

NET  U1_C2_DDR3_CKE             LOC =  L13; # Bank  36
NET  U1_C2_DDR3_CS_B            LOC =  D16; # Bank  36

NET  U1_C2_DDR3_A13             LOC =  R15; # Bank  36
NET  U1_C2_DDR3_A12             LOC =  E13; # Bank  36
NET  U1_C2_DDR3_A11             LOC =  K13; # Bank  36
NET  U1_C2_DDR3_A10             LOC =  D13; # Bank  36
NET  U1_C2_DDR3_A9              LOC =  N14; # Bank  36
NET  U1_C2_DDR3_A8              LOC =  J13; # Bank  36
NET  U1_C2_DDR3_A7              LOC =  T15; # Bank  36
NET  U1_C2_DDR3_A6              LOC =  L15; # Bank  36
NET  U1_C2_DDR3_A5              LOC =  M14; # Bank  36
NET  U1_C2_DDR3_A4              LOC =  G14; # Bank  36
NET  U1_C2_DDR3_A3              LOC =  L14; # Bank  36
NET  U1_C2_DDR3_A2              LOC =  M15; # Bank  36
NET  U1_C2_DDR3_A1              LOC =  H14; # Bank  36
NET  U1_C2_DDR3_A0              LOC =  D15; # Bank  36

NET  U1_C2_DDR3_BA0             LOC =  P13; # Bank  36
NET  U1_C2_DDR3_BA1             LOC =  N13; # Bank  36
NET  U1_C2_DDR3_BA2             LOC =  E16; # Bank  36 (E15 on Rev B)

NET  U1_C2_DDR3_RAS_B           LOC =  H13; # Bank  36
NET  U1_C2_DDR3_CAS_B           LOC =  P15; # Bank  36
NET  U1_C2_DDR3_WE_B            LOC =  P14; # Bank  36
NET  U1_C2_DDR3_ODT             LOC =  F13; # Bank  36
NET  U1_C2_DDR3_RESET_B         LOC =  F14; # Bank  36 (E16 on Rev B)
##
##  Byte lane 0
##
NET  U1_C2_DDR3_DQS0_P          LOC =  C32; # Bank  26
```

```
NET  U1_C2_DDR3_DQS0_N          LOC =  C33; # Bank  26
NET  U1_C2_DDR3_DQ0             LOC =  D30; # Bank  26
NET  U1_C2_DDR3_DQ1             LOC =  B31; # Bank  26
NET  U1_C2_DDR3_DQ2             LOC =  E30; # Bank  26
NET  U1_C2_DDR3_DQ3             LOC =  B30; # Bank  26
NET  U1_C2_DDR3_DQ4             LOC =  M31; # Bank  26
NET  U1_C2_DDR3_DQ5             LOC =  A30; # Bank  26
NET  U1_C2_DDR3_DQ6             LOC =  M30; # Bank  26
NET  U1_C2_DDR3_DQ7             LOC =  A32; # Bank  26
##
##  Byte lane 1
##
NET  U1_C2_DDR3_DQS1_P          LOC =  N29; # Bank  26
NET  U1_C2_DDR3_DQS1_N          LOC =  M29; # Bank  26
NET  U1_C2_DDR3_DQ8             LOC =  D31; # Bank  26
NET  U1_C2_DDR3_DQ9             LOC =  A33; # Bank  26
NET  U1_C2_DDR3_DQ10            LOC =  F32; # Bank  26
NET  U1_C2_DDR3_DQ11            LOC =  B32; # Bank  26
NET  U1_C2_DDR3_DQ12            LOC =  H32; # Bank  26
NET  U1_C2_DDR3_DQ13            LOC =  P29; # Bank  26
NET  U1_C2_DDR3_DQ14            LOC =  G31; # Bank  26
NET  U1_C2_DDR3_DQ15            LOC =  C31; # Bank  26
##
##  Byte lane 2
##
NET  U1_C2_DDR3_DQS2_P          LOC =  R30; # Bank  26
NET  U1_C2_DDR3_DQS2_N          LOC =  P30; # Bank  26
NET  U1_C2_DDR3_DQ16            LOC =  E32; # Bank  26
NET  U1_C2_DDR3_DQ17            LOC =  K32; # Bank  26
NET  U1_C2_DDR3_DQ18            LOC =  H31; # Bank  26
NET  U1_C2_DDR3_DQ19            LOC =  K31; # Bank  26
NET  U1_C2_DDR3_DQ20            LOC =  F30; # Bank  26
NET  U1_C2_DDR3_DQ21            LOC =  L30; # Bank  26
NET  U1_C2_DDR3_DQ22            LOC =  G30; # Bank  26
NET  U1_C2_DDR3_DQ23            LOC =  L32; # Bank  26
##
##  Byte lane 3
##
NET  U1_C2_DDR3_DQS3_P          LOC =  G15; # Bank  36
NET  U1_C2_DDR3_DQS3_N          LOC =  F15; # Bank  36
NET  U1_C2_DDR3_DQ24            LOC =  C14; # Bank  36
NET  U1_C2_DDR3_DQ25            LOC =  B14; # Bank  36
NET  U1_C2_DDR3_DQ26            LOC =  A17; # Bank  36
NET  U1_C2_DDR3_DQ27            LOC =  A14; # Bank  36
NET  U1_C2_DDR3_DQ28            LOC =  D14; # Bank  36
NET  U1_C2_DDR3_DQ29            LOC =  A15; # Bank  36
NET  U1_C2_DDR3_DQ30            LOC =  C16; # Bank  36
NET  U1_C2_DDR3_DQ31            LOC =  B15; # Bank  36
##
## MIG Reserved CCIO "P" NC Pins
##
NET  No Connect                 LOC =  R28; # Bank  26 MRCC
NET  No Connect                 LOC =  J31; # Bank  26 MRCC
NET  No Connect                 LOC =  E31; # Bank  26 SRCC
NET  No Connect                 LOC =  E15; # Bank  36 SRCC
NET  No Connect                 LOC =  J14; # Bank  36 SRCC (Rev C)
```

```
##########################################
##
##  32-bit DDR3 Controller C1
##
##########################################

NET  U1_C1_DDR3_CLK_P          LOC =  R16; # Bank  37
NET  U1_C1_DDR3_CLK_N          LOC =  P16; # Bank  37

NET  U1_C1_DDR3_CKE            LOC =  L17; # Bank  37
NET  U1_C1_DDR3_CS_B           LOC =  F18; # Bank  37

NET  U1_C1_DDR3_A13            LOC =  N16; # Bank  37
NET  U1_C1_DDR3_A12            LOC =  G16; # Bank  37
NET  U1_C1_DDR3_A11            LOC =  K17; # Bank  37
NET  U1_C1_DDR3_A10            LOC =  D18; # Bank  37
NET  U1_C1_DDR3_A9             LOC =  M17; # Bank  37
NET  U1_C1_DDR3_A8             LOC =  K16; # Bank  37
NET  U1_C1_DDR3_A7             LOC =  N17; # Bank  37
NET  U1_C1_DDR3_A6             LOC =  J16; # Bank  37
NET  U1_C1_DDR3_A5             LOC =  R17; # Bank  37
NET  U1_C1_DDR3_A4             LOC =  H17; # Bank  37
NET  U1_C1_DDR3_A3             LOC =  T17; # Bank  37
NET  U1_C1_DDR3_A2             LOC =  M16; # Bank  37
NET  U1_C1_DDR3_A1             LOC =  H16; # Bank  37
NET  U1_C1_DDR3_A0             LOC =  H19; # Bank  37

NET  U1_C1_DDR3_BA0            LOC =  L18; # Bank  37
NET  U1_C1_DDR3_BA1            LOC =  K18; # Bank  37
NET  U1_C1_DDR3_BA2            LOC =  J19; # Bank  37

NET  U1_C1_DDR3_RAS_B          LOC =  G17; # Bank  37
NET  U1_C1_DDR3_CAS_B          LOC =  P19; # Bank  37 (R18 on Rev B)
NET  U1_C1_DDR3_WE_B           LOC =  P18; # Bank  37
NET  U1_C1_DDR3_ODT            LOC =  N19; # Bank  37
NET  U1_C1_DDR3_RESET_B        LOC =  F19; # Bank  37
##
##  Byte lane 0
##
NET  U1_C1_DDR3_DQS0_P         LOC =  C27; # Bank  27
NET  U1_C1_DDR3_DQS0_N         LOC =  C28; # Bank  27
NET  U1_C1_DDR3_DQ0            LOC =  B27; # Bank  27
NET  U1_C1_DDR3_DQ1            LOC =  E27; # Bank  27
NET  U1_C1_DDR3_DQ2            LOC =  A27; # Bank  27
NET  U1_C1_DDR3_DQ3            LOC =  F27; # Bank  27
NET  U1_C1_DDR3_DQ4            LOC =  A29; # Bank  27
NET  U1_C1_DDR3_DQ5            LOC =  M26; # Bank  27
NET  U1_C1_DDR3_DQ6            LOC =  A28; # Bank  27
NET  U1_C1_DDR3_DQ7            LOC =  N26; # Bank  27
##
##  Byte lane 1
##
NET  U1_C1_DDR3_DQS1_P         LOC =  N27; # Bank  27
NET  U1_C1_DDR3_DQS1_N         LOC =  M27; # Bank  27
NET  U1_C1_DDR3_DQ8            LOC =  D28; # Bank  27
NET  U1_C1_DDR3_DQ9            LOC =  D29; # Bank  27
NET  U1_C1_DDR3_DQ10           LOC =  E28; # Bank  27
NET  U1_C1_DDR3_DQ11           LOC =  B29; # Bank  27
NET  U1_C1_DDR3_DQ12           LOC =  F28; # Bank  27
```

```
NET  U1_C1_DDR3_DQ13            LOC =  F29; # Bank  27
NET  U1_C1_DDR3_DQ14            LOC =  P25; # Bank  27
NET  U1_C1_DDR3_DQ15            LOC =  C29; # Bank  27
##
##  Byte lane 2
##
NET  U1_C1_DDR3_DQS2_P          LOC =  P28; # Bank  27
NET  U1_C1_DDR3_DQS2_N          LOC =  N28; # Bank  27
NET  U1_C1_DDR3_DQ16            LOC =  L28; # Bank  27
NET  U1_C1_DDR3_DQ17            LOC =  K27; # Bank  27
NET  U1_C1_DDR3_DQ18            LOC =  G27; # Bank  27
NET  U1_C1_DDR3_DQ19            LOC =  K26; # Bank  27
NET  U1_C1_DDR3_DQ20            LOC =  L29; # Bank  27
NET  U1_C1_DDR3_DQ21            LOC =  K28; # Bank  27
NET  U1_C1_DDR3_DQ22            LOC =  H28; # Bank  27
NET  U1_C1_DDR3_DQ23            LOC =  L27; # Bank  27
##
##  Byte lane 3
##
NET  U1_C1_DDR3_DQS3_P          LOC =  M19; # Bank  37
NET  U1_C1_DDR3_DQS3_N          LOC =  L19; # Bank  37
NET  U1_C1_DDR3_DQ24            LOC =  C19; # Bank  37
NET  U1_C1_DDR3_DQ25            LOC =  C17; # Bank  37
NET  U1_C1_DDR3_DQ26            LOC =  E18; # Bank  37
NET  U1_C1_DDR3_DQ27            LOC =  E17; # Bank  37
NET  U1_C1_DDR3_DQ28            LOC =  G19; # Bank  37
NET  U1_C1_DDR3_DQ29            LOC =  C18; # Bank  37
NET  U1_C1_DDR3_DQ30            LOC =  F17; # Bank  37
NET  U1_C1_DDR3_DQ31            LOC =  D19; # Bank  37
##
## MIG Reserved CCIO "P" NC Pins
##
NET  No Connect                 LOC =  R25; # Bank  27 MRCC
NET  No Connect                 LOC =  G29; # Bank  27 MRCC
NET  No Connect                 LOC =  H27; # Bank  27 SRCC
NET  No Connect                 LOC =  H19; # Bank  37 SRCC
NET  No Connect                 LOC =  R18; # Bank  37 MRCC (Rev C)

##########################################
##
##  32-bit DDR3 Controller C0
##
##########################################


NET  U1_C0_DDR3_CLK_P           LOC =  K21; # Bank  38
NET  U1_C0_DDR3_CLK_N           LOC =  J20; # Bank  38

NET  U1_C0_DDR3_CKE             LOC =  P21; # Bank  38
NET  U1_C0_DDR3_CS_B            LOC =  A22; # Bank  38

NET  U1_C0_DDR3_A13             LOC =  R21; # Bank  38
NET  U1_C0_DDR3_A12             LOC =  G20; # Bank  38
NET  U1_C0_DDR3_A11             LOC =  E20; # Bank  38
NET  U1_C0_DDR3_A10             LOC =  R22; # Bank  38
NET  U1_C0_DDR3_A9              LOC =  K20; # Bank  38
NET  U1_C0_DDR3_A8              LOC =  G22; # Bank  38
NET  U1_C0_DDR3_A7              LOC =  R23; # Bank  38
NET  U1_C0_DDR3_A6              LOC =  D20; # Bank  38
```

```
NET  U1_C0_DDR3_A5              LOC =  L20; # Bank  38
NET  U1_C0_DDR3_A4              LOC =  F22; # Bank  38
NET  U1_C0_DDR3_A3              LOC =  R20; # Bank  38
NET  U1_C0_DDR3_A2              LOC =  H21; # Bank  38
NET  U1_C0_DDR3_A1              LOC =  F20; # Bank  38
NET  U1_C0_DDR3_A0              LOC =  P20; # Bank  38

NET  U1_C0_DDR3_BA0             LOC =  H22; # Bank  38
NET  U1_C0_DDR3_BA1             LOC =  G21; # Bank  38
NET  U1_C0_DDR3_BA2             LOC =  E21; # Bank  38

NET  U1_C0_DDR3_RAS_B           LOC =  A20; # Bank  38
NET  U1_C0_DDR3_CAS_B           LOC =  M20; # Bank  38 (N22 Rev B)
NET  U1_C0_DDR3_WE_B            LOC =  N21; # Bank  38
NET  U1_C0_DDR3_ODT             LOC =  M21; # Bank  38 (M20 on Rev B)
NET  U1_C0_DDR3_RESET_B         LOC =  B22; # Bank  38
##
##  Byte lane 0
##
NET  U1_C0_DDR3_DQS0_P          LOC =  C26; # Bank  28
NET  U1_C0_DDR3_DQS0_N          LOC =  B26; # Bank  28
NET  U1_C0_DDR3_DQ0             LOC =  F23; # Bank  28
NET  U1_C0_DDR3_DQ1             LOC =  F24; # Bank  28
NET  U1_C0_DDR3_DQ2             LOC =  E23; # Bank  28
NET  U1_C0_DDR3_DQ3             LOC =  D24; # Bank  28
NET  U1_C0_DDR3_DQ4             LOC =  L23; # Bank  28
NET  U1_C0_DDR3_DQ5             LOC =  D23; # Bank  28
NET  U1_C0_DDR3_DQ6             LOC =  K23; # Bank  28
NET  U1_C0_DDR3_DQ7             LOC =  C24; # Bank  28
##
##  Byte lane 1
##
NET  U1_C0_DDR3_DQS1_P          LOC =  L24; # Bank  28
NET  U1_C0_DDR3_DQS1_N          LOC =  L25; # Bank  28
NET  U1_C0_DDR3_DQ8             LOC =  A25; # Bank  28
NET  U1_C0_DDR3_DQ9             LOC =  A24; # Bank  28
NET  U1_C0_DDR3_DQ10            LOC =  B25; # Bank  28
NET  U1_C0_DDR3_DQ11            LOC =  A23; # Bank  28
NET  U1_C0_DDR3_DQ12            LOC =  D25; # Bank  28
NET  U1_C0_DDR3_DQ13            LOC =  M25; # Bank  28
NET  U1_C0_DDR3_DQ14            LOC =  C23; # Bank  28
NET  U1_C0_DDR3_DQ15            LOC =  B24; # Bank  28
##
##  Byte lane 2
##
NET  U1_C0_DDR3_DQS2_P          LOC =  P23; # Bank  28
NET  U1_C0_DDR3_DQS2_N          LOC =  P24; # Bank  28
NET  U1_C0_DDR3_DQ16            LOC =  J24; # Bank  28
NET  U1_C0_DDR3_DQ17            LOC =  G26; # Bank  28
NET  U1_C0_DDR3_DQ18            LOC =  H23; # Bank  28
NET  U1_C0_DDR3_DQ19            LOC =  D26; # Bank  28
NET  U1_C0_DDR3_DQ20            LOC =  J23; # Bank  28
NET  U1_C0_DDR3_DQ22            LOC =  H24; # Bank  28
NET  U1_C0_DDR3_DQ21            LOC =  G24; # Bank  28
NET  U1_C0_DDR3_DQ23            LOC =  G25; # Bank  28
##
##  Byte lane 3
##
NET  U1_C0_DDR3_DQS3_P          LOC =  M22; # Bank  38
```

```
NET  U1_C0_DDR3_DQS3_N          LOC =  L22; # Bank  38
NET  U1_C0_DDR3_DQ24            LOC =  A19; # Bank  38
NET  U1_C0_DDR3_DQ25            LOC =  B19; # Bank  38
NET  U1_C0_DDR3_DQ26            LOC =  C21; # Bank  38
NET  U1_C0_DDR3_DQ27            LOC =  E22; # Bank  38
NET  U1_C0_DDR3_DQ28            LOC =  J21; # Bank  38
NET  U1_C0_DDR3_DQ29            LOC =  A18; # Bank  38
NET  U1_C0_DDR3_DQ30            LOC =  C22; # Bank  38
NET  U1_C0_DDR3_DQ31            LOC =  B20; # Bank  38
##
## MIG Reserved NC Pins
##
NET  No Connect                 LOC =  M24; # Bank  28 - MRCC
NET  No Connect                 LOC =  E25; # Bank  28 - MRCC
NET  No Connect                 LOC =  E26; # Bank  28 - SRCC
NET  No Connect                 LOC =  B21; # Bank  38 - SRCC
NET  No Connect                 LOC =  N22; # Bank  38 - MRCC (Rev C)
```

Appendix C

ML631 Master UCF Listing for U2

The ML631 master user constraints file (UCF) template provides for designs targeting the ML631 Virtex-6 HXT FPGA Packet Processor/Traffic Manager evaluation board. Net names in the constraints listed in this appendix correlate with net names on the *ML631 Schematic* [Ref 1]. Users must identify the appropriate pins and replace the net names in this appendix with net names in the user RTL. See UG625, *Constraints Guide*, for more information [Ref 3].

```
##########################################################################
##
##  ML631 REV C PIN LISTING: INITIAL RELEASE
##
##  FPGA U2: HX565T-2FFG1923C
##
##  Note: Memory designs must use internal VREF for any bank
##        with SSTL15 inputs.
##        Example: CONFIG INTERNAL_VREF_BANK34=0.75;
##
##  Note: All FPGA banks are 1.5V
##
##  Note: Banks 22 and 32 are DCI masters (for DCI cascade)
##
##########################################################################
##
## User LEDS
##
NET  U2_USER_LED6              LOC = BA14 ; #
NET  U2_USER_LED5              LOC = BA13 ; #
NET  U2_USER_LED4              LOC = AM21 ; #
NET  U2_USER_LED3              LOC = AN21 ; #
NET  U2_USER_LED2              LOC = AY15 ; #
NET  U2_USER_LED1              LOC = BA15 ; #
##
## User Pushbutton switches:
##
NET  U2_USER_PB4               LOC = BB14 ; #
NET  U2_USER_PB3               LOC = BC14 ; #
NET  U2_USER_PB2               LOC = BC18 ; #
NET  U2_USER_PB1               LOC = BD18 ; #
##
## CP2103 USB-to-UART interface:
##
NET  U2_USB_LS_CTS_I_B         LOC = AT20 ; #
NET  U2_USB_LS_RTS_0_B         LOC = AU20 ; #
NET  U2_USB_LS_RXD_I           LOC = AP23 ; #
NET  U2_USB_LS_TXD_0           LOC = AR23 ; #
```

```
##
## I2C interface
##
NET  U2_SDA_MAIN                LOC = K25  ; #
NET  U2_SCL_MAIN                LOC = J25  ; #

############################
##
## Global clock inputs
##
############################

NET  U2_LVDS_OSC_P              LOC = R31  ; # 200MHz
NET  U2_LVDS_OSC_N              LOC = R32  ; #
NET  U2_SI570_4_P               LOC = J33  ; # 156.25MHz I2C @0x5D
NET  U2_SI570_4_N               LOC = H33  ; #
NET  U2_SI570_5_P               LOC = N12  ; # 156.25MHz I2C @0x5D
NET  U2_SI570_5_N               LOC = M12  ; #

############################################
##
## Interlaken General Purpose I/O Signals
## 1.5V to 3.3V level shifters on PCB
##
############################################

## J4 flow control signals
NET  U2_AMR4_FC_LS_SYNC         LOC = AT24 ; #
NET  U2_AMR4_FC_LS_DATA         LOC = AU24 ; #
NET  U2_AMR4_FC_LS_CK           LOC = AN24 ; #

## P4 flow control signals
NET  U2_AMH4_FC_LS_SYNC         LOC = AP24 ; #
NET  U2_AMH4_FC_LS_DATA         LOC = BA24 ; #
NET  U2_AMH4_FC_LS_CK           LOC = BB24 ; #

## P4 I/O controls:
NET  U2_AMH4_LS_IO7             LOC = AV23 ; #
NET  U2_AMH4_LS_IO6             LOC = AW23 ; #
NET  U2_AMH4_LS_IO5             LOC = AW21 ; #
NET  U2_AMH4_LS_IO4             LOC = AY21 ; #
NET  U2_AMH4_LS_IO3             LOC = AN23 ; #
NET  U2_AMH4_LS_IO2             LOC = AN22 ; #
NET  U2_AMH4_LS_IO1             LOC = AU21 ; #
NET  U2_AMH4_LS_IO0             LOC = AV21 ; #

##########################
##
## Chip to chip I/O
## Single ended 1.5V
##
##########################
NET  U1_U2_C2CIO20              LOC = B31  ; #
NET  U1_U2_C2CIO19              LOC = A32  ; #
NET  U1_U2_C2CIO18              LOC = AY11 ; #
NET  U1_U2_C2CIO17              LOC = AT28 ; #
NET  U1_U2_C2CIO16              LOC = BD29 ; #
NET  U1_U2_C2CIO15              LOC = N18  ; #
NET  U1_U2_C2CIO14              LOC = N17  ; #
```

```
NET  U1_U2_C2CIO13              LOC = H17  ; #
NET  U1_U2_C2CIO12              LOC = G16  ; #
NET  U1_U2_C2CIO11              LOC = J16  ; #
NET  U1_U2_C2CIO10              LOC = H16  ; #
NET  U1_U2_C2CIO9               LOC = T17  ; #
NET  U1_U2_C2CIO8               LOC = R17  ; #
NET  U1_U2_C2CIO7               LOC = N16  ; #
NET  U1_U2_C2CIO6               LOC = M16  ; #
NET  U1_U2_C2CIO5               LOC = K17  ; #
NET  U1_U2_C2CIO4               LOC = K16  ; #
NET  U1_U2_C2CIO3               LOC = M17  ; #
NET  U1_U2_C2CIO2               LOC = L17  ; #
NET  U1_U2_C2CIO1               LOC = R16  ; #
NET  U1_U2_C2CIO0               LOC = P16  ; #


###################################
##
## 16-bit DDR3 Controller C0
##
###################################
##
## DDR3 C0 clocks:
##
NET  U2_C0_DDR3_CLK_P           LOC = AL34 ; #
NET  U2_C0_DDR3_CLK_N           LOC = AM35 ; #
##
## DDR3 C0 controls:
##
NET  U2_C0_DDR3_CS_B            LOC = BB34 ; #
NET  U2_C0_DDR3_CKE             LOC = BA35 ; #
NET  U2_C0_DDR3_ODT             LOC = BB35 ; #
NET  U2_C0_DDR3_RESET_B         LOC = AL35 ; #
NET  U2_C0_DDR3_RAS_B           LOC = AW35 ; #
NET  U2_C0_DDR3_CAS_B           LOC = AY35 ; #
NET  U2_C0_DDR3_WE_B            LOC = AY33 ; #
##
## DDR3 C0 addresses:
##
NET  U2_C0_DDR3_A13             LOC = AP34 ; #
NET  U2_C0_DDR3_A12             LOC = AT34 ; #
NET  U2_C0_DDR3_A11             LOC = AN33 ; #
NET  U2_C0_DDR3_A10             LOC = AU34 ; #
NET  U2_C0_DDR3_A9              LOC = AT33 ; #
NET  U2_C0_DDR3_A8              LOC = AP33 ; #
NET  U2_C0_DDR3_A7              LOC = AP35 ; #
NET  U2_C0_DDR3_A6              LOC = AR35 ; #
NET  U2_C0_DDR3_A5              LOC = AH32 ; #
NET  U2_C0_DDR3_A4              LOC = AR33 ; #
NET  U2_C0_DDR3_A3              LOC = AK33 ; #
NET  U2_C0_DDR3_A2              LOC = AH33 ; #
NET  U2_C0_DDR3_A1              LOC = AT35 ; #
NET  U2_C0_DDR3_A0              LOC = AJ33 ; #
##
## DDR3 C0 bank addresses:
##
NET  U2_C0_DDR3_BA2             LOC = AV34 ; #
NET  U2_C0_DDR3_BA1             LOC = AV33 ; #
NET  U2_C0_DDR3_BA0             LOC = AW34 ; #
```

```
##
## DDR3 C0 byte group 0:
##
NET  U2_C0_DDR3_LDQS_P          LOC = AK11 ; #
NET  U2_C0_DDR3_LDQS_N          LOC = AK10 ; #
NET  U2_C0_DDR3_LDM             LOC = AM11 ; #
NET  U2_C0_DDR3_DQ7             LOC = AL13 ; #
NET  U2_C0_DDR3_DQ6             LOC = AH13 ; #
NET  U2_C0_DDR3_DQ5             LOC = AK13 ; #
NET  U2_C0_DDR3_DQ4             LOC = AL10 ; #
NET  U2_C0_DDR3_DQ3             LOC = AM12 ; #
NET  U2_C0_DDR3_DQ2             LOC = AH12 ; #
NET  U2_C0_DDR3_DQ1             LOC = AL12 ; #
NET  U2_C0_DDR3_DQ0             LOC = AK12 ; #
##
## DDR3 C0 byte group 1:
##
NET  U2_C0_DDR3_UDQS_P          LOC = AT9  ; #
NET  U2_C0_DDR3_UDQS_N          LOC = AT8  ; #
NET  U2_C0_DDR3_UDM             LOC = AT5  ; #
NET  U2_C0_DDR3_DQ15            LOC = AU1  ; #
NET  U2_C0_DDR3_DQ14            LOC = AJ13 ; #
NET  U2_C0_DDR3_DQ13            LOC = AU5  ; #
NET  U2_C0_DDR3_DQ12            LOC = AR6  ; #
NET  U2_C0_DDR3_DQ11            LOC = AT7  ; #
NET  U2_C0_DDR3_DQ10            LOC = AJ14 ; #
NET  U2_C0_DDR3_DQ9             LOC = AU2  ; #
NET  U2_C0_DDR3_DQ8             LOC = AP10 ; #
##
## Bank 34 NC pins for MIG:
##
NET  No Connect                 LOC = AN11 ; # SRCC_34
NET  No Connect                 LOC = AU6  ; # SRCC_34


####################################
##
## 16-bit DDR3 Controller C1
##
####################################
##
## DDR3 C1 clocks:
##
NET  U2_C1_DDR3_CLK_P           LOC = AJ29 ; #
NET  U2_C1_DDR3_CLK_N           LOC = AK30 ; #
##
## DDR3 C1 controls:
##
NET  U2_C1_DDR3_CS_B            LOC = BB32 ; #
NET  U2_C1_DDR3_CKE             LOC = AY32 ; #
NET  U2_C1_DDR3_ODT             LOC = BA32 ; #
NET  U2_C1_DDR3_RESET_B         LOC = AV31 ; #
NET  U2_C1_DDR3_RAS_B           LOC = BA30 ; #
NET  U2_C1_DDR3_CAS_B           LOC = BB30 ; #
NET  U2_C1_DDR3_WE_B            LOC = AU31 ; #
##
## DDR3 C1 addresses:
##
NET  U2_C1_DDR3_A13             LOC = AL32 ; #
```

```
NET  U2_C1_DDR3_A12             LOC = AJ31 ; #
NET  U2_C1_DDR3_A11             LOC = AR32 ; #
NET  U2_C1_DDR3_A10             LOC = AJ30 ; #
NET  U2_C1_DDR3_A9              LOC = AN32 ; #
NET  U2_C1_DDR3_A8              LOC = AR31 ; #
NET  U2_C1_DDR3_A7              LOC = AV32 ; #
NET  U2_C1_DDR3_A6              LOC = AT30 ; #
NET  U2_C1_DDR3_A5              LOC = AU32 ; #
NET  U2_C1_DDR3_A4              LOC = AP30 ; #
NET  U2_C1_DDR3_A3              LOC = AK31 ; #
NET  U2_C1_DDR3_A2              LOC = AN31 ; #
NET  U2_C1_DDR3_A1              LOC = AR30 ; #
NET  U2_C1_DDR3_A0              LOC = AP31 ; #
##
## DDR3 C1 bank addresses:
##
NET  U2_C1_DDR3_BA2             LOC = AT32 ; #
NET  U2_C1_DDR3_BA1             LOC = AW31 ; #
NET  U2_C1_DDR3_BA0             LOC = AY31 ; #
##
## DDR3 C1 byte group 0:
##
NET  U2_C1_DDR3_LDQS_P          LOC = AK17 ; #
NET  U2_C1_DDR3_LDQS_N          LOC = AK16 ; #
NET  U2_C1_DDR3_LDM             LOC = AN12 ; #
NET  U2_C1_DDR3_DQ7             LOC = AL14 ; #
NET  U2_C1_DDR3_DQ6             LOC = AJ16 ; #
NET  U2_C1_DDR3_DQ5             LOC = AL15 ; #
NET  U2_C1_DDR3_DQ4             LOC = AK15 ; #
NET  U2_C1_DDR3_DQ3             LOC = AM14 ; #
NET  U2_C1_DDR3_DQ2             LOC = AU9  ; #
NET  U2_C1_DDR3_DQ1             LOC = AN13 ; #
NET  U2_C1_DDR3_DQ0             LOC = AJ15 ; #
##
## DDR3 C1 byte group 1:
##
NET  U2_C1_DDR3_UDQS_P          LOC = AP11 ; #
NET  U2_C1_DDR3_UDQS_N          LOC = AR11 ; #
NET  U2_C1_DDR3_UDM             LOC = AV11 ; #
NET  U2_C1_DDR3_DQ15            LOC = AN14 ; #
NET  U2_C1_DDR3_DQ14            LOC = AW8  ; #
NET  U2_C1_DDR3_DQ13            LOC = AM15 ; #
NET  U2_C1_DDR3_DQ12            LOC = AW6  ; #
NET  U2_C1_DDR3_DQ11            LOC = AR12 ; #
NET  U2_C1_DDR3_DQ10            LOC = AY8  ; #
NET  U2_C1_DDR3_DQ9             LOC = AU10 ; #
NET  U2_C1_DDR3_DQ8             LOC = AW9  ; #
##
## Bank 33 NC pins for MIG:
##
NET  No Connect                 LOC = AV7  ; # SRCC_33
NET  No Connect                 LOC = AP13 ; # MRCC_33
NET  No Connect                 LOC = AU11 ; # MRCC_33
NET  No Connect                 LOC = AV9  ; # SRCC_33


####################################
##
## 16-bit DDR3 Controller C2
```

```
##
###################################
##
## DDR3 C2 clocks:
##
NET  U2_C2_DDR3_CLK_P          LOC = AJ26 ; #
NET  U2_C2_DDR3_CLK_N          LOC = AK27 ; #
##
## DDR3 C2 controls:
##
NET  U2_C2_DDR3_CS_B           LOC = BC29 ; #
NET  U2_C2_DDR3_CKE            LOC = BA29 ; #
NET  U2_C2_DDR3_ODT            LOC = BB29 ; #
NET  U2_C2_DDR3_RESET_B        LOC = AW28 ; #
NET  U2_C2_DDR3_RAS_B          LOC = AU27 ; #
NET  U2_C2_DDR3_CAS_B          LOC = AV27 ; #
NET  U2_C2_DDR3_WE_B           LOC = AV28 ; #
##
## DDR3 C2 addresses:
##
NET  U2_C2_DDR3_A13            LOC = AW29 ; #
NET  U2_C2_DDR3_A12            LOC = AJ28 ; #
NET  U2_C2_DDR3_A11            LOC = AN28 ; #
NET  U2_C2_DDR3_A10            LOC = AP28 ; #
NET  U2_C2_DDR3_A9             LOC = AN29 ; #
NET  U2_C2_DDR3_A8             LOC = AR27 ; #
NET  U2_C2_DDR3_A7             LOC = AV29 ; #
NET  U2_C2_DDR3_A6             LOC = AL28 ; #
NET  U2_C2_DDR3_A5             LOC = AT29 ; #
NET  U2_C2_DDR3_A4             LOC = AL27 ; #
NET  U2_C2_DDR3_A3             LOC = AR28 ; #
NET  U2_C2_DDR3_A2             LOC = AP29 ; #
NET  U2_C2_DDR3_A1             LOC = AK28 ; #
NET  U2_C2_DDR3_A0             LOC = AU29 ; #
##
## DDR3 C2 bank addresses:
##
NET  U2_C2_DDR3_BA2            LOC = AT27 ; #
NET  U2_C2_DDR3_BA1            LOC = AY28 ; #
NET  U2_C2_DDR3_BA0            LOC = BA28 ; #
##
##
## DDR3 C2 byte group 0
##
NET  U2_C2_DDR3_LDQS_P         LOC = BB7  ; #
NET  U2_C2_DDR3_LDQS_N         LOC = BB6  ; #
NET  U2_C2_DDR3_LDM            LOC = BA7  ; #
NET  U2_C2_DDR3_DQ7            LOC = BA9  ; #
NET  U2_C2_DDR3_DQ6            LOC = AY10 ; #
NET  U2_C2_DDR3_DQ5            LOC = BB10 ; #
NET  U2_C2_DDR3_DQ4            LOC = BA8  ; #
NET  U2_C2_DDR3_DQ3            LOC = BB9  ; #
NET  U2_C2_DDR3_DQ2            LOC = AY12 ; #
NET  U2_C2_DDR3_DQ1            LOC = BC9  ; #
NET  U2_C2_DDR3_DQ0            LOC = BA10 ; #
##
## DDR3 C2 byte group 1
##
NET  U2_C2_DDR3_UDQS_P         LOC = AW5  ; #
```

```
NET  U2_C2_DDR3_UDQS_N          LOC = AY5  ; #
NET  U2_C2_DDR3_UDM             LOC = BC3  ; #
NET  U2_C2_DDR3_DQ15            LOC = BA4  ; #
NET  U2_C2_DDR3_DQ14            LOC = BC7  ; #
NET  U2_C2_DDR3_DQ13            LOC = BA3  ; #
NET  U2_C2_DDR3_DQ12            LOC = BD6  ; #
NET  U2_C2_DDR3_DQ11            LOC = AY3  ; #
NET  U2_C2_DDR3_DQ10            LOC = BB11 ; #
NET  U2_C2_DDR3_DQ9             LOC = BB4  ; #
NET  U2_C2_DDR3_DQ8             LOC = BA12 ; #
##
## Bank 32 MIG NC pins
##
NET  No Connect                 LOC = BB5  ; # SRCC_32
NET  No Connect                 LOC = BC6  ; # MRCC_32
NET  No Connect                 LOC = BC8  ; # MRCC_32
NET  No Connect                 LOC = BA5  ; # SRCC_32


####################################
##
##  16-bit DDR3 Controller C3
##
####################################
##
## DDR3 C3 clocks:
##
NET  U2_C3_DDR3_CLK_P           LOC = N33  ; #
NET  U2_C3_DDR3_CLK_N           LOC = N34  ; #
##
## DDR3 C3 controls:
##
NET  U2_C3_DDR3_CS_B            LOC = N32  ; #
NET  U2_C3_DDR3_CKE             LOC = F35  ; #
NET  U2_C3_DDR3_RESET_B         LOC = G35  ; #
NET  U2_C3_DDR3_ODT             LOC = P31  ; #
NET  U2_C3_DDR3_RAS_B           LOC = D34  ; #
NET  U2_C3_DDR3_CAS_B           LOC = M35  ; #
NET  U2_C3_DDR3_WE_B            LOC = L35  ; #
##
## DDR3 C3 addresses:
##
NET  U2_C3_DDR3_A13             LOC = B35  ; #
NET  U2_C3_DDR3_A12             LOC = B36  ; #
NET  U2_C3_DDR3_A11             LOC = A37  ; #
NET  U2_C3_DDR3_A10             LOC = P35  ; #
NET  U2_C3_DDR3_A9              LOC = B37  ; #
NET  U2_C3_DDR3_A8              LOC = P34  ; #
NET  U2_C3_DDR3_A7              LOC = L33  ; #
NET  U2_C3_DDR3_A6              LOC = K33  ; #
NET  U2_C3_DDR3_A5              LOC = A35  ; #
NET  U2_C3_DDR3_A4              LOC = J35  ; #
NET  U2_C3_DDR3_A3              LOC = E35  ; #
NET  U2_C3_DDR3_A2              LOC = D35  ; #
NET  U2_C3_DDR3_A1              LOC = K35  ; #
NET  U2_C3_DDR3_A0              LOC = A34  ; #
##
## DDR3 C3 bank addresses:
##
```

```
NET  U2_C3_DDR3_BA2             LOC = C34  ; #
NET  U2_C3_DDR3_BA1             LOC = B34  ; #
NET  U2_C3_DDR3_BA0             LOC = D33  ; #
##
## DDR3 C3 data group 0:
##
NET  U2_C3_DDR3_LDQS_P          LOC = B11  ; #
NET  U2_C3_DDR3_LDQS_N          LOC = A10  ; #
NET  U2_C3_DDR3_LDM             LOC = B12  ; #
NET  U2_C3_DDR3_DQ7             LOC = R12  ; #
NET  U2_C3_DDR3_DQ6             LOC = A13  ; #
NET  U2_C3_DDR3_DQ5             LOC = R13  ; #
NET  U2_C3_DDR3_DQ4             LOC = C12  ; #
NET  U2_C3_DDR3_DQ3             LOC = C13  ; #
NET  U2_C3_DDR3_DQ2             LOC = C11  ; #
NET  U2_C3_DDR3_DQ1             LOC = B9   ; #
NET  U2_C3_DDR3_DQ0             LOC = A12  ; #
##
## DDR3 C3 data group 1:
##
NET  U2_C3_DDR3_UDQS_P          LOC = B10  ; #
NET  U2_C3_DDR3_UDQS_N          LOC = A9   ; #
NET  U2_C3_DDR3_UDM             LOC = E11  ; #
NET  U2_C3_DDR3_DQ15            LOC = E10  ; #
NET  U2_C3_DDR3_DQ14            LOC = J11  ; #
NET  U2_C3_DDR3_DQ13            LOC = D11  ; #
NET  U2_C3_DDR3_DQ12            LOC = F10  ; #
NET  U2_C3_DDR3_DQ11            LOC = H11  ; #
NET  U2_C3_DDR3_DQ10            LOC = J10  ; #
NET  U2_C3_DDR3_DQ9             LOC = F12  ; #
NET  U2_C3_DDR3_DQ8             LOC = G10  ; #
##
## Bank 35 NC pins for MIG
NET  No Connect                 LOC = E12  ; # SRCC_35
NET  No Connect                 LOC = K11  ; # MRCC_35
NET  No Connect                 LOC = G12  ; # MRCC_35
NET  No Connect                 LOC = K10  ; # SRCC_35


####################################
##
## 36-bit QDR-II+ Controller C0
##
####################################
##
## QDR2 C0 Addresses:
##
NET  U2_C0_QDR2_A18             LOC = F23  ; #
NET  U2_C0_QDR2_A17             LOC = F24  ; #
NET  U2_C0_QDR2_A16             LOC = E23  ; #
NET  U2_C0_QDR2_A15             LOC = D24  ; #
NET  U2_C0_QDR2_A14             LOC = C26  ; #
NET  U2_C0_QDR2_A13             LOC = B26  ; #
NET  U2_C0_QDR2_A12             LOC = L23  ; #
NET  U2_C0_QDR2_A11             LOC = K23  ; #
NET  U2_C0_QDR2_A10             LOC = D23  ; #
NET  U2_C0_QDR2_A9              LOC = C24  ; #
NET  U2_C0_QDR2_A8              LOC = C23  ; #
NET  U2_C0_QDR2_A7              LOC = B24  ; #
```

```
NET  U2_C0_QDR2_A6              LOC = L24  ; #
NET  U2_C0_QDR2_A5              LOC = L25  ; #
NET  U2_C0_QDR2_A4              LOC = B25  ; #
NET  U2_C0_QDR2_A3              LOC = A25  ; #
NET  U2_C0_QDR2_A2              LOC = A23  ; #
NET  U2_C0_QDR2_A1              LOC = A24  ; #
NET  U2_C0_QDR2_A0              LOC = M24  ; #
##
## Controls
##
NET  U2_C0_QDR2_WPS_B           LOC = M25  ; #
NET  U2_C0_QDR2_RPS_B           LOC = E25  ; #
NET  U2_C0_QDR2_DOFF_B          LOC = D25  ; #
##
## Read clocks:
##
NET  U2_C0_QDR2_CQ              LOC = N22  ; #
NET  U2_C0_QDR2_CQ_B            LOC = H22  ; #
##
## QDR2 C0 Read byte group 0
##
NET  U2_C0_QDR2_Q0              LOC = C22  ; #
NET  U2_C0_QDR2_Q1              LOC = C21  ; #
NET  U2_C0_QDR2_Q2              LOC = E22  ; #
NET  U2_C0_QDR2_Q3              LOC = D21  ; #
NET  U2_C0_QDR2_Q4              LOC = M22  ; #
NET  U2_C0_QDR2_Q5              LOC = L22  ; #
NET  U2_C0_QDR2_Q6              LOC = B19  ; #
NET  U2_C0_QDR2_Q7              LOC = A18  ; #
NET  U2_C0_QDR2_Q8              LOC = B20  ; #
##
## QDR2 C0 Read byte group 1
##
NET  U2_C0_QDR2_Q9              LOC = A19  ; #
NET  U2_C0_QDR2_Q10             LOC = M21  ; #
NET  U2_C0_QDR2_Q11             LOC = M20  ; #
NET  U2_C0_QDR2_Q12             LOC = B22  ; #
NET  U2_C0_QDR2_Q13             LOC = A22  ; #
NET  U2_C0_QDR2_Q14             LOC = B21  ; #
NET  U2_C0_QDR2_Q15             LOC = A20  ; #
NET  U2_C0_QDR2_Q16             LOC = N21  ; #
NET  U2_C0_QDR2_Q17             LOC = G21  ; #
##
## QDR2 C0 Read byte group 2
##
NET  U2_C0_QDR2_Q18             LOC = E21  ; #
NET  U2_C0_QDR2_Q19             LOC = D20  ; #
NET  U2_C0_QDR2_Q20             LOC = R20  ; #
NET  U2_C0_QDR2_Q21             LOC = P20  ; #
NET  U2_C0_QDR2_Q22             LOC = G22  ; #
NET  U2_C0_QDR2_Q23             LOC = F22  ; #
NET  U2_C0_QDR2_Q24             LOC = L20  ; #
NET  U2_C0_QDR2_Q25             LOC = K20  ; #
NET  U2_C0_QDR2_Q26             LOC = R23  ; #
##
## QDR2 C0 Read byte group 3
##
NET  U2_C0_QDR2_Q27             LOC = R22  ; #
NET  U2_C0_QDR2_Q28             LOC = F20  ; #
```

```
NET  U2_C0_QDR2_Q29             LOC = E20  ; #
NET  U2_C0_QDR2_Q30             LOC = H21  ; #
NET  U2_C0_QDR2_Q31             LOC = G20  ; #
NET  U2_C0_QDR2_Q32             LOC = R21  ; #
NET  U2_C0_QDR2_Q33             LOC = P21  ; #
NET  U2_C0_QDR2_Q34             LOC = K21  ; #
NET  U2_C0_QDR2_Q35             LOC = J20  ; #
##
## QDR2 C0 write clocks
##
NET  U2_C0_QDR2_K               LOC = E26  ; #
NET  U2_C0_QDR2_K_B             LOC = D26  ; #
##
## QDR2 C0 write byte group 0
##
NET  U2_C0_QDR2_BWS0_B          LOC = C28  ; #
NET  U2_C0_QDR2_D0              LOC = B27  ; #
NET  U2_C0_QDR2_D1              LOC = A27  ; #
NET  U2_C0_QDR2_D2              LOC = A28  ; #
NET  U2_C0_QDR2_D3              LOC = A29  ; #
NET  U2_C0_QDR2_D4              LOC = C27  ; #
NET  U2_C0_QDR2_D5              LOC = N26  ; #
NET  U2_C0_QDR2_D6              LOC = M26  ; #
NET  U2_C0_QDR2_D7              LOC = F27  ; #
NET  U2_C0_QDR2_D8              LOC = E27  ; #
##
## QDR2 C0 write byte group 1
##
NET  U2_C0_QDR2_BWS1_B          LOC = E28  ; #
NET  U2_C0_QDR2_D9              LOC = C29  ; #
NET  U2_C0_QDR2_D10             LOC = B29  ; #
NET  U2_C0_QDR2_D11             LOC = N27  ; #
NET  U2_C0_QDR2_D12             LOC = M27  ; #
NET  U2_C0_QDR2_D13             LOC = F28  ; #
NET  U2_C0_QDR2_D14             LOC = D28  ; #
NET  U2_C0_QDR2_D15             LOC = D29  ; #
NET  U2_C0_QDR2_D16             LOC = R25  ; #
NET  U2_C0_QDR2_D17             LOC = P25  ; #
##
## QDR2 C0 write byte group 2
##
NET  U2_C0_QDR2_BWS2_B          LOC = P26  ; #
NET  U2_C0_QDR2_D18             LOC = G29  ; #
NET  U2_C0_QDR2_D19             LOC = F29  ; #
NET  U2_C0_QDR2_D20             LOC = H27  ; #
NET  U2_C0_QDR2_D21             LOC = G27  ; #
NET  U2_C0_QDR2_D22             LOC = R26  ; #
NET  U2_C0_QDR2_D23             LOC = K26  ; #
NET  U2_C0_QDR2_D24             LOC = K27  ; #
NET  U2_C0_QDR2_D25             LOC = L27  ; #
NET  U2_C0_QDR2_D26             LOC = K28  ; #
##
## QDR2 C0 write byte group 3
##
NET  U2_C0_QDR2_BWS3_B          LOC = H29  ; #
NET  U2_C0_QDR2_D27             LOC = P28  ; #
NET  U2_C0_QDR2_D28             LOC = N28  ; #
NET  U2_C0_QDR2_D29             LOC = L28  ; #
NET  U2_C0_QDR2_D30             LOC = L29  ; #
```

```
NET  U2_C0_QDR2_D31             LOC = H28  ; #
NET  U2_C0_QDR2_D32             LOC = T27  ; #
NET  U2_C0_QDR2_D33             LOC = R27  ; #
NET  U2_C0_QDR2_D34             LOC = J28  ; #
NET  U2_C0_QDR2_D35             LOC = J29  ; #


##################################
##
##  36-bit QDR-II+ Controller C1
##
##################################
##
## QDR2 C1 addresses:
##
NET  U2_C1_QDR2_A18             LOC = H19  ; #
NET  U2_C1_QDR2_A17             LOC = G19  ; #
NET  U2_C1_QDR2_A16             LOC = D19  ; #
NET  U2_C1_QDR2_A15             LOC = C19  ; #
NET  U2_C1_QDR2_A14             LOC = E18  ; #
NET  U2_C1_QDR2_A13             LOC = D18  ; #
NET  U2_C1_QDR2_A12             LOC = M19  ; #
NET  U2_C1_QDR2_A11             LOC = L19  ; #
NET  U2_C1_QDR2_A10             LOC = F17  ; #
NET  U2_C1_QDR2_A9              LOC = E17  ; #
NET  U2_C1_QDR2_A8              LOC = C18  ; #
NET  U2_C1_QDR2_A7              LOC = C17  ; #
NET  U2_C1_QDR2_A6              LOC = P19  ; #
NET  U2_C1_QDR2_A5              LOC = N19  ; #
NET  U2_C1_QDR2_A4              LOC = F19  ; #
NET  U2_C1_QDR2_A3              LOC = F18  ; #
NET  U2_C1_QDR2_A2              LOC = H18  ; #
NET  U2_C1_QDR2_A1              LOC = G17  ; #
NET  U2_C1_QDR2_A0              LOC = R18  ; #
##
## QDR2 C1 controls:
##
NET  U2_C1_QDR2_WPS_B           LOC = P18  ; #
NET  U2_C1_QDR2_RPS_B           LOC = L18  ; #
NET  U2_C1_QDR2_DOFF_B          LOC = K18  ; #
##
## QDR2 C1 read clocks:
##
NET  U2_C1_QDR2_CQ              LOC = R28  ; #
NET  U2_C1_QDR2_CQ_B            LOC = J31  ; #
##
## QDR2 C1 read byte group 0
##
NET  U2_C1_QDR2_Q0              LOC = B30  ; #
NET  U2_C1_QDR2_Q1              LOC = A30  ; #
NET  U2_C1_QDR2_Q2              LOC = C32  ; #
NET  U2_C1_QDR2_Q3              LOC = C33  ; #
NET  U2_C1_QDR2_Q4              LOC = M30  ; #
NET  U2_C1_QDR2_Q5              LOC = M31  ; #
NET  U2_C1_QDR2_Q6              LOC = E30  ; #
NET  U2_C1_QDR2_Q7              LOC = D30  ; #
NET  U2_C1_QDR2_Q8              LOC = B32  ; #
##
```

```
## QDR2 C1 read byte group 1
##
NET  U2_C1_QDR2_Q9              LOC = A33  ; #
NET  U2_C1_QDR2_Q10             LOC = N29  ; #
NET  U2_C1_QDR2_Q11             LOC = M29  ; #
NET  U2_C1_QDR2_Q12             LOC = D31  ; #
NET  U2_C1_QDR2_Q13             LOC = C31  ; #
NET  U2_C1_QDR2_Q14             LOC = G31  ; #
NET  U2_C1_QDR2_Q15             LOC = F32  ; #
NET  U2_C1_QDR2_Q16             LOC = P29  ; #
NET  U2_C1_QDR2_Q17             LOC = H32  ; #
##
## QDR2 C1 read byte group 2
##
NET  U2_C1_QDR2_Q18             LOC = E31  ; #
NET  U2_C1_QDR2_Q19             LOC = E32  ; #
NET  U2_C1_QDR2_Q20             LOC = N31  ; #
NET  U2_C1_QDR2_Q21             LOC = M32  ; #
NET  U2_C1_QDR2_Q22             LOC = G30  ; #
NET  U2_C1_QDR2_Q23             LOC = F30  ; #
NET  U2_C1_QDR2_Q24             LOC = L30  ; #
NET  U2_C1_QDR2_Q25             LOC = K31  ; #
NET  U2_C1_QDR2_Q26             LOC = R30  ; #
##
## QDR2 C1 read byte group 3
##
NET  U2_C1_QDR2_Q27             LOC = P30  ; #
NET  U2_C1_QDR2_Q28             LOC = L32  ; #
NET  U2_C1_QDR2_Q29             LOC = K32  ; #
NET  U2_C1_QDR2_Q30             LOC = H31  ; #
NET  U2_C1_QDR2_Q31             LOC = G32  ; #
NET  U2_C1_QDR2_Q32             LOC = T29  ; #
NET  U2_C1_QDR2_Q33             LOC = T30  ; #
NET  U2_C1_QDR2_Q34             LOC = K30  ; #
NET  U2_C1_QDR2_Q35             LOC = J30  ; #
##
## QDR2 C1 write clocks
##
NET  U2_C1_QDR2_K               LOC = J19  ; #
NET  U2_C1_QDR2_K_B             LOC = J18  ; #
##
## QDR2 C1 write byte group 0
##
NET  U2_C1_QDR2_BWS0_B          LOC = B16  ; #
NET  U2_C1_QDR2_D0              LOC = B17  ; #
NET  U2_C1_QDR2_D1              LOC = A17  ; #
NET  U2_C1_QDR2_D2              LOC = B15  ; #
NET  U2_C1_QDR2_D3              LOC = A15  ; #
NET  U2_C1_QDR2_D4              LOC = C16  ; #
NET  U2_C1_QDR2_D5              LOC = G15  ; #
NET  U2_C1_QDR2_D6              LOC = F15  ; #
NET  U2_C1_QDR2_D7              LOC = D14  ; #
NET  U2_C1_QDR2_D8              LOC = C14  ; #
##
## QDR2 C1 write byte group 1
##
NET  U2_C1_QDR2_BWS1_B          LOC = D16  ; #
NET  U2_C1_QDR2_D9              LOC = B14  ; #
NET  U2_C1_QDR2_D10             LOC = A14  ; #
```

```
NET  U2_C1_QDR2_D11             LOC = F14  ; #
NET  U2_C1_QDR2_D12             LOC = F13  ; #
NET  U2_C1_QDR2_D13             LOC = E16  ; #
NET  U2_C1_QDR2_D14             LOC = J14  ; #
NET  U2_C1_QDR2_D15             LOC = H13  ; #
NET  U2_C1_QDR2_D16             LOC = P15  ; #
NET  U2_C1_QDR2_D17             LOC = P14  ; #
##
## QDR2 C1 write byte group 2
##
NET  U2_C1_QDR2_BWS2_B          LOC = M14  ; #
NET  U2_C1_QDR2_D18             LOC = P13  ; #
NET  U2_C1_QDR2_D19             LOC = N13  ; #
NET  U2_C1_QDR2_D20             LOC = E15  ; #
NET  U2_C1_QDR2_D21             LOC = D15  ; #
NET  U2_C1_QDR2_D22             LOC = N14  ; #
NET  U2_C1_QDR2_D23             LOC = H14  ; #
NET  U2_C1_QDR2_D24             LOC = G14  ; #
NET  U2_C1_QDR2_D25             LOC = K13  ; #
NET  U2_C1_QDR2_D26             LOC = J13  ; #
##
## QDR2 C1 write byte group 3
##
NET  U2_C1_QDR2_BWS3_B          LOC = D13  ; #
NET  U2_C1_QDR2_D27             LOC = T15  ; #
NET  U2_C1_QDR2_D28             LOC = R15  ; #
NET  U2_C1_QDR2_D29             LOC = M15  ; #
NET  U2_C1_QDR2_D30             LOC = L15  ; #
NET  U2_C1_QDR2_D31             LOC = E13  ; #
NET  U2_C1_QDR2_D32             LOC = L14  ; #
NET  U2_C1_QDR2_D33             LOC = L13  ; #
NET  U2_C1_QDR2_D34             LOC = K15  ; #
NET  U2_C1_QDR2_D35             LOC = J15  ; #


####################################
##
##  DDR2 SRAM Controller C0
##
####################################
##
## Write clocks:
##
NET  U2_C0_DDR2_SRAM_K          LOC = AY27 ; #
NET  U2_C0_DDR2_SRAM_K_B        LOC = BA27 ; #
##
## Controls:
##
NET  U2_C0_DDR2_SRAM_DOFF_B     LOC = AJ24 ; #
NET  U2_C0_DDR2_SRAM_LD_B       LOC = AK25 ; #
NET  U2_C0_DDR2_SRAM_R_WE_B     LOC = BC28 ; #
##
## Addresses:
##
NET  U2_C0_DDR2_SRAM_A19        LOC = BD28 ; #
NET  U2_C0_DDR2_SRAM_A18        LOC = AM31 ; #
NET  U2_C0_DDR2_SRAM_A17        LOC = AM32 ; #
NET  U2_C0_DDR2_SRAM_A16        LOC = AU30 ; #
```

```
NET  U2_C0_DDR2_SRAM_A15        LOC = BC32 ; #
NET  U2_C0_DDR2_SRAM_A14        LOC = AL30 ; #
NET  U2_C0_DDR2_SRAM_A13        LOC = AM30 ; #
NET  U2_C0_DDR2_SRAM_A12        LOC = BD30 ; #
NET  U2_C0_DDR2_SRAM_A11        LOC = BD31 ; #
NET  U2_C0_DDR2_SRAM_A10        LOC = AW30 ; #
NET  U2_C0_DDR2_SRAM_A9         LOC = AY30 ; #
NET  U2_C0_DDR2_SRAM_A8         LOC = AL29 ; #
NET  U2_C0_DDR2_SRAM_A7         LOC = AM29 ; #
NET  U2_C0_DDR2_SRAM_A6         LOC = BB31 ; #
NET  U2_C0_DDR2_SRAM_A5         LOC = BC31 ; #
NET  U2_C0_DDR2_SRAM_A4         LOC = H34  ; #
NET  U2_C0_DDR2_SRAM_A3         LOC = AM27 ; #
NET  U2_C0_DDR2_SRAM_A2         LOC = AN27 ; #
NET  U2_C0_DDR2_SRAM_A1         LOC = BB27 ; #
NET  U2_C0_DDR2_SRAM_A0         LOC = BC27 ; #
##
## DDR2 C0 SRAM Read Clocks:
##
NET  U2_C0_DDR2_SRAM_CQ_B       LOC = AK35 ; #
NET  U2_C0_DDR2_SRAM_CQ         LOC = AW33 ; #
##
NET  U2_C0_DDR2_SRAM_QVLD       LOC = AM34 ; #
##
## Lower byte group:
##
NET  U2_C0_DDR2_SRAM_BWS0_B     LOC = BC34 ; #
NET  U2_C0_DDR2_SRAM_DQ8        LOC = AN34 ; #
NET  U2_C0_DDR2_SRAM_DQ7        LOC = BD34 ; #
NET  U2_C0_DDR2_SRAM_DQ6        LOC = BD35 ; #
NET  U2_C0_DDR2_SRAM_DQ5        LOC = BA33 ; #
NET  U2_C0_DDR2_SRAM_DQ4        LOC = BA34 ; #
NET  U2_C0_DDR2_SRAM_DQ3        LOC = AK32 ; #
NET  U2_C0_DDR2_SRAM_DQ2        LOC = AL33 ; #
NET  U2_C0_DDR2_SRAM_DQ1        LOC = BC33 ; #
NET  U2_C0_DDR2_SRAM_DQ0        LOC = BD33 ; #
##
## Upper byte group:
##
NET  U2_C0_DDR2_SRAM_BWS1_B     LOC = AU35 ; #
NET  U2_C0_DDR2_SRAM_DQ17       LOC = F33  ; #
NET  U2_C0_DDR2_SRAM_DQ16       LOC = E33  ; #
NET  U2_C0_DDR2_SRAM_DQ15       LOC = G34  ; #
NET  U2_C0_DDR2_SRAM_DQ14       LOC = F34  ; #
NET  U2_C0_DDR2_SRAM_DQ13       LOC = R33  ; #
NET  U2_C0_DDR2_SRAM_DQ12       LOC = P33  ; #
NET  U2_C0_DDR2_SRAM_DQ11       LOC = M34  ; #
NET  U2_C0_DDR2_SRAM_DQ10       LOC = L34  ; #
NET  U2_C0_DDR2_SRAM_DQ9        LOC = J34  ; #


####################################
##
##  DDR2 SRAM Controller C1
##
####################################
##
## DDR2 SRAM C1 write clocks:
##
```

```
NET  U2_C1_DDR2_SRAM_K_B        LOC = BC4  ; #
NET  U2_C1_DDR2_SRAM_K          LOC = BD3  ; #
##
## DDR2 SRAM C1 controls:
##
NET  U2_C1_DDR2_SRAM_DOFF_B     LOC = BC2  ; #
NET  U2_C1_DDR2_SRAM_LD_B       LOC = BB2  ; #
NET  U2_C1_DDR2_SRAM_R_WE_B     LOC = BB1  ; #
NET  U2_C1_DDR2_SRAM_QVLD       LOC = A8   ; #
##
## DDR2 SRAM C1 addresses:
NET  U2_C1_DDR2_SRAM_A19        LOC = AY2  ; #
NET  U2_C1_DDR2_SRAM_A18        LOC = BA2  ; #
NET  U2_C1_DDR2_SRAM_A17        LOC = BD5  ; #
NET  U2_C1_DDR2_SRAM_A16        LOC = BD4  ; #
NET  U2_C1_DDR2_SRAM_A15        LOC = AW1  ; #
NET  U2_C1_DDR2_SRAM_A14        LOC = AY1  ; #
NET  U2_C1_DDR2_SRAM_A13        LOC = AP14 ; #
NET  U2_C1_DDR2_SRAM_A12        LOC = AR13 ; #
NET  U2_C1_DDR2_SRAM_A11        LOC = AV8  ; #
NET  U2_C1_DDR2_SRAM_A10        LOC = AW10 ; #
NET  U2_C1_DDR2_SRAM_A9         LOC = AU7  ; #
NET  U2_C1_DDR2_SRAM_A8         LOC = AV6  ; #
NET  U2_C1_DDR2_SRAM_A7         LOC = AL17 ; #
NET  U2_C1_DDR2_SRAM_A6         LOC = AM16 ; #
NET  U2_C1_DDR2_SRAM_A5         LOC = AY7  ; #
NET  U2_C1_DDR2_SRAM_A4         LOC = AY6  ; #
NET  U2_C1_DDR2_SRAM_A3         LOC = AV12 ; #
NET  U2_C1_DDR2_SRAM_A2         LOC = AW11 ; #
NET  U2_C1_DDR2_SRAM_A1         LOC = AT12 ; #
NET  U2_C1_DDR2_SRAM_A0         LOC = AU12 ; #
##
## Read clocks:
##
NET  U2_C1_DDR2_SRAM_CQ         LOC = AR8  ; #
NET  U2_C1_DDR2_SRAM_CQ_B       LOC = AR7  ; #
##
## DDR2 SRAM C1 byte group 0:
##
NET  U2_C1_DDR2_SRAM_BWS0_B     LOC = P10  ; #
NET  U2_C1_DDR2_SRAM_DQ8        LOC = D10  ; #
NET  U2_C1_DDR2_SRAM_DQ7        LOC = M11  ; #
NET  U2_C1_DDR2_SRAM_DQ6        LOC = L10  ; #
NET  U2_C1_DDR2_SRAM_DQ5        LOC = L12  ; #
NET  U2_C1_DDR2_SRAM_DQ4        LOC = K12  ; #
NET  U2_C1_DDR2_SRAM_DQ3        LOC = H12  ; #
NET  U2_C1_DDR2_SRAM_DQ2        LOC = G11  ; #
NET  U2_C1_DDR2_SRAM_DQ1        LOC = N11  ; #
NET  U2_C1_DDR2_SRAM_DQ0        LOC = M10  ; #
##
## DDR2 SRAM C1 byte group 1:
##
NET  U2_C1_DDR2_SRAM_BWS1_B     LOC = P11  ; #
NET  U2_C1_DDR2_SRAM_DQ17       LOC = AU4  ; #
NET  U2_C1_DDR2_SRAM_DQ16       LOC = AV2  ; #
NET  U2_C1_DDR2_SRAM_DQ15       LOC = AV1  ; #
NET  U2_C1_DDR2_SRAM_DQ14       LOC = AW4  ; #
NET  U2_C1_DDR2_SRAM_DQ13       LOC = AW3  ; #
NET  U2_C1_DDR2_SRAM_DQ12       LOC = AV4  ; #
```

```
NET  U2_C1_DDR2_SRAM_DQ11       LOC = AV3  ; #
NET  U2_C1_DDR2_SRAM_DQ10       LOC = AR10 ; #
NET  U2_C1_DDR2_SRAM_DQ9        LOC = AT10 ; #


########################################
##
## U138 NetLogic MicroSystems NL9K
##
########################################
##
## U138 NL clocks:
##
NET  NL_CLK                     LOC = AT3  ; #
NET  NL_CLK_B                   LOC = AT2  ; #
NET  NL_DCLK0                   LOC = BC13 ; #
NET  NL_DCLK0_B                 LOC = BC12 ; #
NET  NL_DCLK1                   LOC = AT14 ; #
NET  NL_DCLK1_B                 LOC = AT13 ; #
NET  NL_DCLK2                   LOC = AV24 ; #
NET  NL_DCLK2_B                 LOC = AW24 ; #
##
## U138 NL9K resets:
##
NET  NL_SRST_B                  LOC = AR5  ; #
NET  NL_CRST_B                  LOC = AT4  ; #
##
## U138 NL9K miscellaneous:
##
NET  NL_PEO_B                   LOC = AM10 ; #
NET  NL_PHSE0_B                 LOC = K22  ; #
NET  NL_GIO_B                   LOC = J21  ; #
##
## U138 NL9K Data Valids:
##
NET  NL_DV_2                    LOC = BD24 ; #
NET  NL_DV_1                    LOC = AY13 ; #
NET  NL_DV_0                    LOC = AU16 ; #
##
## U138 NL9K Parity
##
NET  NL_DPR_0                   LOC = AT17 ; #
NET  NL_DPR_1                   LOC = BB16 ; #
##
## DBUS(79:0)
##
NET  NL_DBUS00                  LOC = AT25 ; #
NET  NL_DBUS01                  LOC = AU25 ; #
NET  NL_DBUS02                  LOC = AM26 ; #
NET  NL_DBUS03                  LOC = AN26 ; #
NET  NL_DBUS04                  LOC = AW26 ; #
NET  NL_DBUS05                  LOC = AY26 ; #
NET  NL_DBUS06                  LOC = AJ23 ; #
NET  NL_DBUS07                  LOC = AK23 ; #
NET  NL_DBUS08                  LOC = BA25 ; #
NET  NL_DBUS09                  LOC = BB25 ; #
NET  NL_DBUS10                  LOC = AU26 ; #
NET  NL_DBUS11                  LOC = AV26 ; #
NET  NL_DBUS12                  LOC = AK22 ; #
```

```
NET  NL_DBUS13                LOC = AL23 ; #
NET  NL_DBUS14                LOC = AW25 ; #
NET  NL_DBUS15                LOC = AY25 ; #
NET  NL_DBUS16                LOC = AP26 ; #
NET  NL_DBUS17                LOC = AR26 ; #
NET  NL_DBUS19                LOC = AL22 ; #
NET  NL_DBUS18                LOC = AM22 ; #
NET  NL_DBUS20                LOC = BB26 ; #
NET  NL_DBUS21                LOC = BC26 ; #
NET  NL_DBUS22                LOC = AP25 ; #
NET  NL_DBUS23                LOC = AR25 ; #
NET  NL_DBUS24                LOC = AL25 ; #
NET  NL_DBUS25                LOC = AM25 ; #
NET  NL_DBUS26                LOC = BD25 ; #
NET  NL_DBUS27                LOC = BD26 ; #
NET  NL_DBUS28                LOC = AL24 ; #
NET  NL_DBUS29                LOC = AM24 ; #
NET  NL_DBUS30                LOC = BC24 ; #
NET  NL_DBUS31                LOC = AN16 ; #
NET  NL_DBUS32                LOC = AP15 ; #
NET  NL_DBUS33                LOC = AL18 ; #
NET  NL_DBUS34                LOC = AM17 ; #
NET  NL_DBUS35                LOC = AP16 ; #
NET  NL_DBUS36                LOC = AR16 ; #
NET  NL_DBUS37                LOC = AJ21 ; #
NET  NL_DBUS38                LOC = AK21 ; #
NET  NL_DBUS39                LOC = AN18 ; #
NET  NL_DBUS40                LOC = AN17 ; #
NET  NL_DBUS41                LOC = AM19 ; #
NET  NL_DBUS42                LOC = AN19 ; #
NET  NL_DBUS43                LOC = AJ18 ; #
NET  NL_DBUS44                LOC = AK18 ; #
NET  NL_DBUS45                LOC = AP18 ; #
NET  NL_DBUS46                LOC = AR17 ; #
NET  NL_DBUS47                LOC = AR15 ; #
NET  NL_DBUS48                LOC = AT15 ; #
NET  NL_DBUS50                LOC = AJ20 ; #
NET  NL_DBUS49                LOC = AJ19 ; #
NET  NL_DBUS51                LOC = AU15 ; #
NET  NL_DBUS52                LOC = AV14 ; #
NET  NL_DBUS53                LOC = AK20 ; #
NET  NL_DBUS54                LOC = AL19 ; #
NET  NL_DBUS55                LOC = AW15 ; #
NET  NL_DBUS56                LOC = AW14 ; #
NET  NL_DBUS57                LOC = AU14 ; #
NET  NL_DBUS58                LOC = AV13 ; #
NET  NL_DBUS59                LOC = AL20 ; #
NET  NL_DBUS60                LOC = AM20 ; #
NET  NL_DBUS61                LOC = AW13 ; #
NET  NL_DBUS62                LOC = AR18 ; #
NET  NL_DBUS63                LOC = AT18 ; #
NET  NL_DBUS64                LOC = AT19 ; #
NET  NL_DBUS65                LOC = AU19 ; #
NET  NL_DBUS66                LOC = AU17 ; #
NET  NL_DBUS67                LOC = AV17 ; #
NET  NL_DBUS68                LOC = AP20 ; #
NET  NL_DBUS69                LOC = AP19 ; #
NET  NL_DBUS70                LOC = BA17 ; #
NET  NL_DBUS71                LOC = BB17 ; #
```

```
NET  NL_DBUS72                LOC = AV18 ; #
NET  NL_DBUS73                LOC = AW18 ; #
NET  NL_DBUS74                LOC = AP21 ; #
NET  NL_DBUS75                LOC = AR20 ; #
NET  NL_DBUS76                LOC = AY18 ; #
NET  NL_DBUS77                LOC = BA18 ; #
NET  NL_DBUS78                LOC = BB12 ; #
NET  NL_DBUS79                LOC = BC11 ; #
##
## U138 NL9K DIBUS(5:0)
##
NET  NL_DIBUS0                LOC = BB15 ; #
NET  NL_DIBUS1                LOC = AV16 ; #
NET  NL_DIBUS2                LOC = AW16 ; #
NET  NL_DIBUS3                LOC = BD11 ; #
NET  NL_DIBUS4                LOC = BD10 ; #
NET  NL_DIBUS5                LOC = BD14 ; #
##
## U138 NL9K DCTX(6:0)
##
NET  NL_DCTX0                 LOC = BD13 ; #
NET  NL_DCTX1                 LOC = AY17 ; #
NET  NL_DCTX2                 LOC = AY16 ; #
NET  NL_DCTX3                 LOC = BC17 ; #
NET  NL_DCTX4                 LOC = BD16 ; #
NET  NL_DCTX5                 LOC = BC16 ; #
NET  NL_DCTX6                 LOC = BD15 ; #
##
## U138 NL9K
## RBUS Interface:
##
NET  NL_RCLK0                 LOC = AY22 ; # MRCC_20
NET  NL_RCLK0_B               LOC = BA22 ; # MRCC_20
##
NET  NL_RV_0                  LOC = AY23 ; #
NET  NL_RPR_0                 LOC = BA23 ; #
##
NET  NL_RBUS00                LOC = BD21 ; #
NET  NL_RBUS01                LOC = BD20 ; #
NET  NL_RBUS02                LOC = BC19 ; #
NET  NL_RBUS03                LOC = BD19 ; #
NET  NL_RBUS04                LOC = BB21 ; #
NET  NL_RBUS05                LOC = BC21 ; #
NET  NL_RBUS06                LOC = AT23 ; #
NET  NL_RBUS07                LOC = AT22 ; #
NET  NL_RBUS08                LOC = BC23 ; #
NET  NL_RBUS09                LOC = BD23 ; #
NET  NL_RBUS10                LOC = BA19 ; #
NET  NL_RBUS11                LOC = BB19 ; #
NET  NL_RBUS12                LOC = AU22 ; #
NET  NL_RBUS13                LOC = AV22 ; #
NET  NL_RBUS14                LOC = AV19 ; #
NET  NL_RBUS15                LOC = AW19 ; #
NET  NL_RBUS16                LOC = BB22 ; #
NET  NL_RBUS17                LOC = BC22 ; #
NET  NL_RBUS19                LOC = AR22 ; #
NET  NL_RBUS18                LOC = AR21 ; #
NET  NL_RBUS20                LOC = BA20 ; #
NET  NL_RBUS21                LOC = BB20 ; #
```

```
NET  NL_RBUS22                  LOC = AW20 ; #
NET  NL_RBUS23                  LOC = AY20 ; #


########################
##
## VGA Debug Header
##
########################

NET  U2_VGA_VSYNC               LOC = J23  ; #
NET  U2_VGA_HSYNC               LOC = H23  ; #
NET  U2_VGA_R_3                 LOC = G25  ; #
NET  U2_VGA_R_2                 LOC = G26  ; #
NET  U2_VGA_R_1                 LOC = P23  ; #
NET  U2_VGA_R_0                 LOC = P24  ; #
NET  U2_VGA_G_3                 LOC = J24  ; #
NET  U2_VGA_G_2                 LOC = H24  ; #
NET  U2_VGA_G_1                 LOC = G24  ; #
NET  U2_VGA_G_0                 LOC = F25  ; #
NET  U2_VGA_B_3                 LOC = N23  ; #
NET  U2_VGA_B_2                 LOC = N24  ; #
NET  U2_VGA_B_1                 LOC = J26  ; #
NET  U2_VGA_B_0                 LOC = H26  ; #
```

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Appendix D

Additional Resources

Xilinx Resources

To search the Answer database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx Support website at:

http://www.xilinx.com/support

For a glossary of technical terms used in Xilinx documentation, see:

http://www.xilinx.com/support/documentation/sw_manuals/glossary.pdf

References

These documents provide supplemental material useful with this user guide:

1. *ML631 Schematic*
   http://www.xilinx.com/support/documentation/ml631.htm
2. DS080, *System ACE CompactFlash Solution*
3. UG625, *Constraints Guide*
4. DS150, *Virtex-6 Family Overview*
5. DS152, *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics*
6. UG360, *Virtex-6 FPGA Configuration User Guide*
7. UG361, *Virtex-6 FPGA SelectIO Resources User Guide*
8. UG362, *Virtex-6 FPGA User Guide: Clocking Resources*
9. UG364, *Virtex-6 FPGA Configurable Logic Block User Guide*
10. UG365, *Virtex-6 FPGA Packaging and Pinout Specifications*
11. UG366, *Virtex-6 FPGA GTX Transceivers User Guide*
12. UG370, *Virtex-6 FPGA System Monitor User Guide*
13. UG371, *Virtex-6 FPGA GTH Transceivers User Guide*
14. DS581, *XPS External Peripheral Controller (EPC) Data Sheet*
15. DS606, *XPS IIC Bus Interface (v2.00a) Data Sheet*

Additional Useful Sites for Boards and Kits

16. General information for the ML631 board and evaluation kit is available at
    http://www.xilinx.com/products/boards-and-kits/EK-V6-ML631-G.htm
17. View and download the latest board schematics, bills of material, reference design files, and user guides
    http://www.xilinx.com/support/documentation/index.htm

Third Party Resources

18. Texas Instruments digital power website
    http://www.ti.com/ww/en/analog/digital-power/index.html
19. Texas Instruments TI SN65LVCP408PAP data sheet
    www.ti.com
20. SiTime SI9102AI oscillator information
    http://www.sitime.com/products/differential-oscillators/sit9102
21. Silicon Labs CP2103 USB-to-UART bridge information
    http://www.silabs.com/products/interface/usbtouart/Pages/default.aspx
22. Silicon Labs home page
    http://www.silabs.com/Pages/default.aspx
23. The Interlaken protocol definition and recommended connector pinouts are in documents located on the Interlaken Alliance website
    http://www.interlakenalliance.com/

    For the Protocol, refer to the *Interlaken Look-Aside Protocol Definition v1.x* and for connector pinouts, refer to *Interlaken Interop Recommendations v1.x*. The protocol definition document also discusses the flow control functions provided by the TX and RX FC_CLK, FC_DATA and FC_SYNC connector pins.
24. ML631 Si570 programming
    http://www.xilinx.com/support/documentation/ml631.htm
25. NetLogic Microsystems processor information
    www.netlogicmicro.com