MultiPRO Desktop Tool

DS114 (v1.9) February 8, 2008 **Product Specification**

This product is undergoing discontinuance. Please refer to XCN07022, *Product Discontinuation Notice*, for more information on last-time purchases and replacement products.

Features

- Supported by ISE™ iMPACT download software (v5.1i SP3 or higher)
- Externally powered using +5V DC power brick
  - Same power brick can be used for Parallel Cable IV
- Download speeds up to 10 Megabits per second (Mb/s)
- LED status indicators
- Uses IEEE 1284 ECP protocol for high-speed communications
- Uses quick-connect, off-the-shelf IEEE 1284 parallel cable
- Power cord options for US/Asia/Japan/Europe/UK

Desktop Device Programming

- Device adapters are available for:
  - XC18V00 ISP PROM family
  - Platform Flash PROM family
  - CoolRunner™-II CPLD family
- Automatically switches power during programming
- Automatically identifies and confirms proper adapter selection
- Has short-circuit protection in the event of improper device insertion

In-System Programming/Configuration

- Automatically senses and adapts to target I/O voltage
- Interfaces to devices operating at 5V (TTL), 3.3V (LVCMOS), 2.5V, 1.8V, and 1.5V
- Supports IEEE 1149.1 (JTAG), serial peripheral interface (SPI), Xilinx Slave-Serial, and Xilinx Slave-SelectMAP (8-bit)
- In-system configures the following Xilinx devices:
  - Virtex™ series FPGAs
  - Spartan™ series FPGAs
  - CoolRunner/CoolRunner-II CPLDs
  - Platform Flash PROM family
  - XC18V00 ISP PROM family
  - XC4000 series FPGAs
  - XC9500/XL/XV CPLDs
- J Drive compatible with IEEE 1532 Programming Engine
- ChipScope™ Pro Analyzer compatible
- Embedded Development Kit (EDK) compatible
- Includes high-performance ribbon cables
  - 14-conductor ribbon cable can be used with Parallel Cable IV
- Intended for development — not recommended for production programming

MultiPRO Desktop Tool Description

The MultiPRO Desktop Tool (Figure 1) is a multi-function programming and configuration cable. When mated with MultiPRO device adapters, it can program individual Platform Flash PROMs, XC18V00 ISP PROMs and CoolRunner-II CPLDs. Alternatively, the tool can perform in-system programming or FPGA configuration when attached to user hardware by way of the included ribbon cables. IEEE 1149.1 (JTAG), serial peripheral interface (SPI), Xilinx Slave-Serial, and Xilinx Slave-SelectMAP (8-bit) protocols are supported in ISP mode.

Designed for use in a desktop environment, the MultiPRO Desktop Tool interfaces to a PC using the industry standard IEEE 1284 parallel port. An external AC power brick provides +5V DC to the pod. An integral power switch facilitates fail-safe connection to target systems.

A variety of device adapters are available for standalone programming of Xilinx Platform Flash PROMs, XC18V00 ISP PROMs, and CoolRunner-II CPLDs.

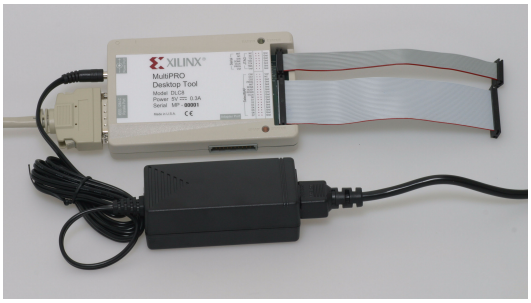

Figure 1: **Xilinx MultiPRO Desktop Tool**

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Device Adapters

A separate device adapter is available for each unique Platform Flash PROM, XC18V00 ISP PROM, and CoolRunner-II CPLD package. Adapters attach to the MultiPRO pod using a 20-pin keyed DIN connector (Figure 2). Power is automatically applied to the adapter during programming operations and removed upon completion. A power status LED is illuminated whenever power is active. The MultiPRO pod automatically identifies any adapter that is attached to the DIN connector.

> ***Caution!*** Devices should never be installed or removed from sockets while the ACTIVE LED is illuminated.

A polycarbonate label protects the top side of the adapter printed circuit. Text clearly identifies the device and package information, the product ordering number, and the index pin locator needed to orient the device during insertion.

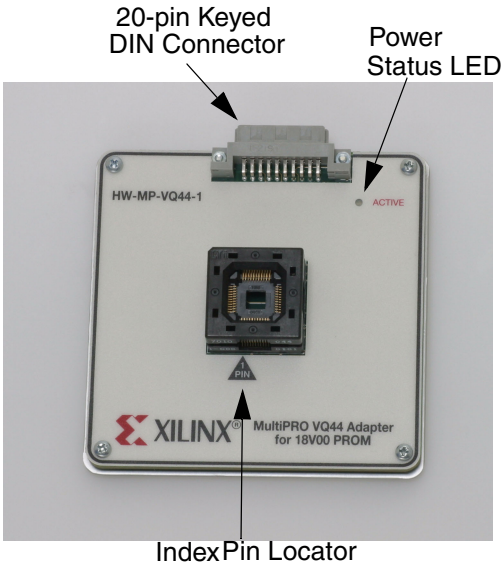


Figure 2: **Common Adapter Features**

An aluminum plate is attached to the bottom side of the printed circuit board to protect circuitry. Rubber feet are mounted on the bottom of the aluminum plate to avoid scratching the desk top.

Over-Current Protection

The MultiPRO Desktop Tool monitors the current load of the adapter when power is provided. If a fault condition exists on the adapter (e.g., if a device is improperly oriented in the socket or the device is internally shorted), power is automatically shut off. The MultiPRO Desktop Tool will not be damaged if the power pins on the DIN connector are inadvertently shorted to ground.

Status Indicators

The MultiPRO Desktop Tool uses tri-color LEDs to indicate the active configuration port and the presence of target power (Table 1). A red LED indicates that the associated port has not been selected in iMPACT. An amber LED indicates that the port is selected but that V_{REF} from the target hardware is not powered. A green LED indicates that the port is selected and V_{REF} from the target hardware is powered.

If both the Serial/JTAG/SPI and SelectMAP STATUS LEDs are red, then the Adapter port is active. Power is automatically switched to adapters only during programming operations. The adapter's red ACTIVE LED is illuminated when power is ON. The MultiPRO Desktop Tool selects the Serial/JTAG/SPI port by default when powered up.

If both the Serial/JTAG/SPI and SelectMAP LEDs are blinking red, an over-current condition has been detected on the adapter port. The adapter should be removed and checked for incorrect device insertion and/or socket damage.

Table 1: **Status Indicators**

Serial/JTAG/SPI LED	SelectMAP LED	Pod Powered	Active Port	V_{REF} Powered	IEEE 1284 Parallel Port Connected
Off	Off	No	None	N/A	Yes
Amber	Red	Yes	S/JTAG	No	Yes
Green	Red	Yes	S/JTAG	Yes	Yes
Red	Amber	Yes	SelectMAP	No	Yes
Red	Green	Yes	SelectMAP	Yes	Yes
Red	Red	Yes	Adapter	See ACTIVE LED	Yes
Blinking Red	Blinking Red	Over-Current	Adapter	N/A	Yes
Amber	Amber	Yes	None	N/A	No

Physical Description

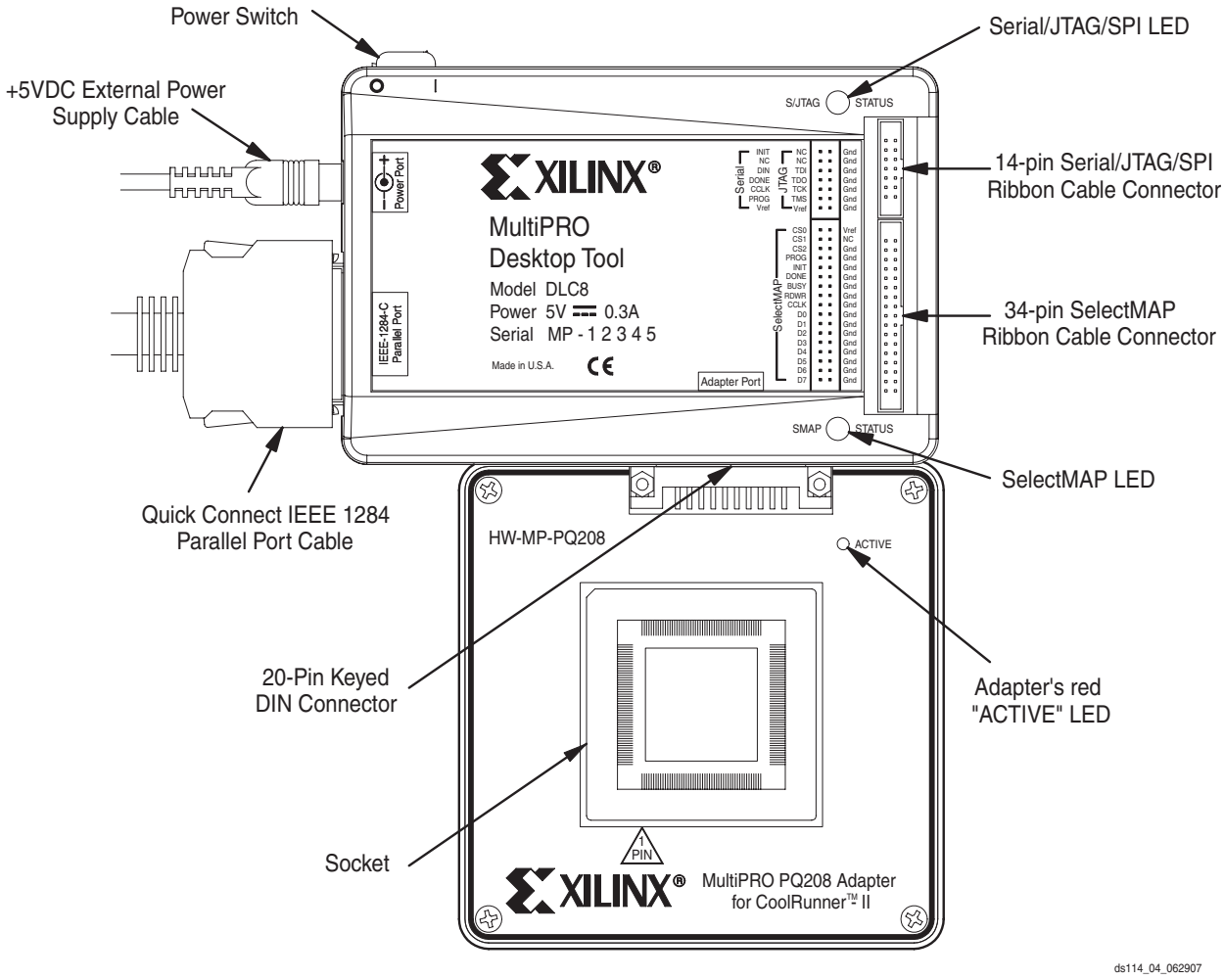


Figure 3: **MultiPRO Connector Descriptions**

External Power Supply

The MultiPRO Desktop Tool requires an external +5V DC power supply. The power supply is a CE approved switching regulator that operates from an AC outlet and connects to the MultiPRO tool using a 5.5 mm x 2.1 mm plug (Figure 4). A power switch on the MultiPRO case is provided as a convenience so that all other cables can remain attached.

The standard MultiPRO power supply (CUI Inc. #DTS050400UC-P5P-KH) is capable of operating from 100VAC to 240VAC at 47 Hz to 63 Hz. The +5V DC output is rated for 4A. This power supply can also be used with the Xilinx Parallel Cable IV (configuration cable) instead of the supplied Power Splitter Cable.

Figure 4: **Standard External +5V DC Power Brick**

IEEE 1284 Cable Specifications

Level 1 compliant host parallel ports are only designed to operate over a maximum cable length of 10 feet. Level 2 compliant ports are designed to operate over a maximum cable length of 33 feet. MultiPRO uses a Level 2 compliant cable interface buffer. The MultiPRO case has an integrated mini-centronics connector for attachment to off-the-shelf IEEE 1284 cables.

Xilinx recommends that the MultiPRO tool be directly connected to the host parallel port without the use of a switch box. Software license "dongles" should not be attached to the parallel port when communicating with the MultiPRO tool.

Automatic Voltage Sensing

The MultiPRO Desktop Tool continuously monitors the V_{REF} pin on the Serial/JTAG/SPI and SelectMAP target interface connectors. The current drain from the target power supply attached to the V_{REF} pin is less than 10 mA at 3.3V DC. The target system reference voltage must be regulated and cannot have a current limiting resistor in series with the V_{REF} pin on the interface.

No damage will occur to the MultiPRO Desktop Tool if the target system is powered when the MultiPRO tool is not powered. However, when powering up a system, it is preferable to apply power to the MultiPRO tool first, followed by power to the target system. The sequence should be reversed when powering down.

The MultiPRO Desktop Tool always puts interface signals on inactive ports in a 3-state condition.

The MultiPRO output drive voltage levels do not linearly track voltage changes on the V_{REF} pin. An appropriate output signal level is established for a range of V_{REF} voltages. For example, if V_{REF} is any voltage from +3.0V DC to +5.0V DC, the MultiPRO tool sets the output signals for the respective port to +3.3V DC.

Refer to Table 2 for the relationship between V_{REF} voltage and MultiPRO output signal levels.

Table 2: **Output Signal Levels as a Function of V_{REF}**

V_{REF} Voltage on Target System	MultiPRO Output Signal Levels	Units
0.80 to 1.65	1.5	V
1.65 to 2.00	1.8	V
2.00 to 3.00	2.5	V
3.00 to 5.00	3.3	V

Connecting to Host Computer

The MultiPRO tool connects to any PC using Windows or Linux[1] through the built-in, standard IEEE 1284 DB25 parallel (printer) port connector[2]. To fully utilize the higher speeds of this cable, the host PC must have a parallel port that is enabled[3] to support extended capability port (ECP) mode. If ECP mode is not enabled, the MultiPRO tool will default to compatibility mode and will not run at the optimum speeds listed. Performance also depends on the MultiPRO Desktop Tool firmware revision and ISE iMPACT software version.[4]

Notes:

1. Refer to ISE software manuals for details regarding supported operating systems.
2. Xilinx makes no representations about compatibility with third-party IEEE 1284 add-on adapters and does not support the add-on adapters.
3. Refer to host PC BIOS to see if ECP mode is enabled.
4. Refer to the MultiPRO Desktop Tool firmware history at http://www.xilinx.com/support/programr/mp_history.htm.

High Performance Ribbon Cable

Two insulation displacement connector (IDC) ribbon cables are supplied and recommended for connection to target systems. See Figure 5 and Figure 6. These cables incorporate multiple signal-ground pairs and facilitate error-free connection. A very small footprint, keyed mating connector is all that is required on the target system. Refer to Figure 7 and Figure 8 for the appropriate connector pin assignments and sample vendor part numbers. The 14-conductor ribbon cable can also be used with Parallel Cable IV.

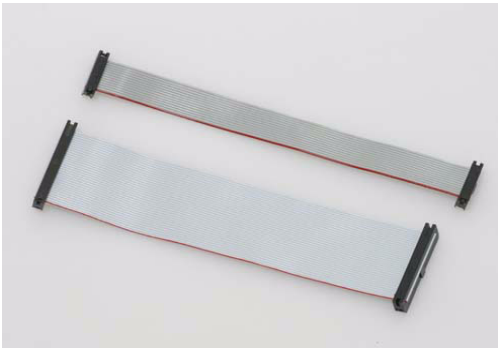
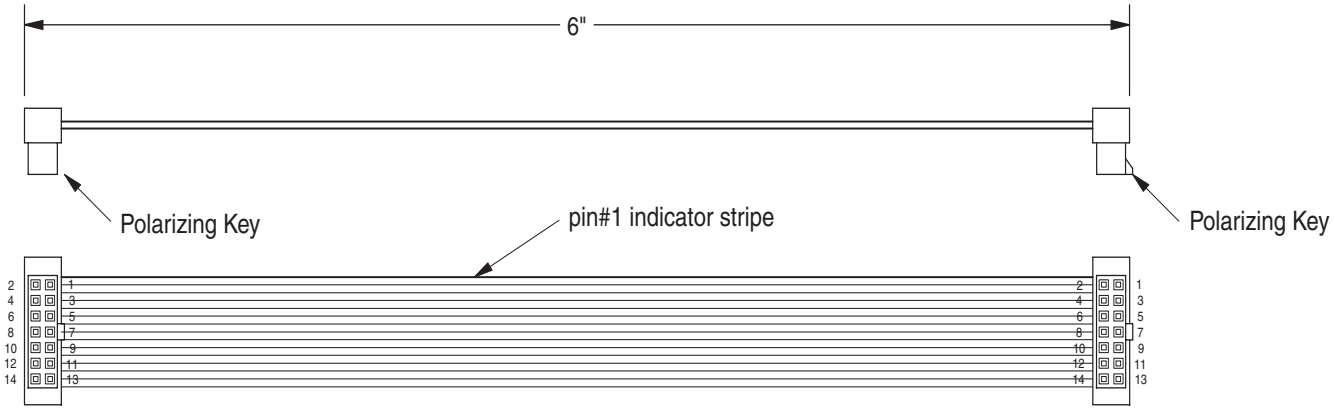


Figure 5: **High Performance Ribbon Cables**



Notes:

1. Ribbon cable – 14-conductor, 1.0 mm centers round conductor flat cable, 28AWG (7x36) stranded copper conductors; gray PVC with pin #1 edge marked.
2. 2 mm ribbon, female polarized connectors – IDC connection to ribbon, contacts are beryllium copper plated with 30 micro inches gold plating over 50 micro inches nickel, connectors mate to 0.5 mm square posts on 2 mm centers.

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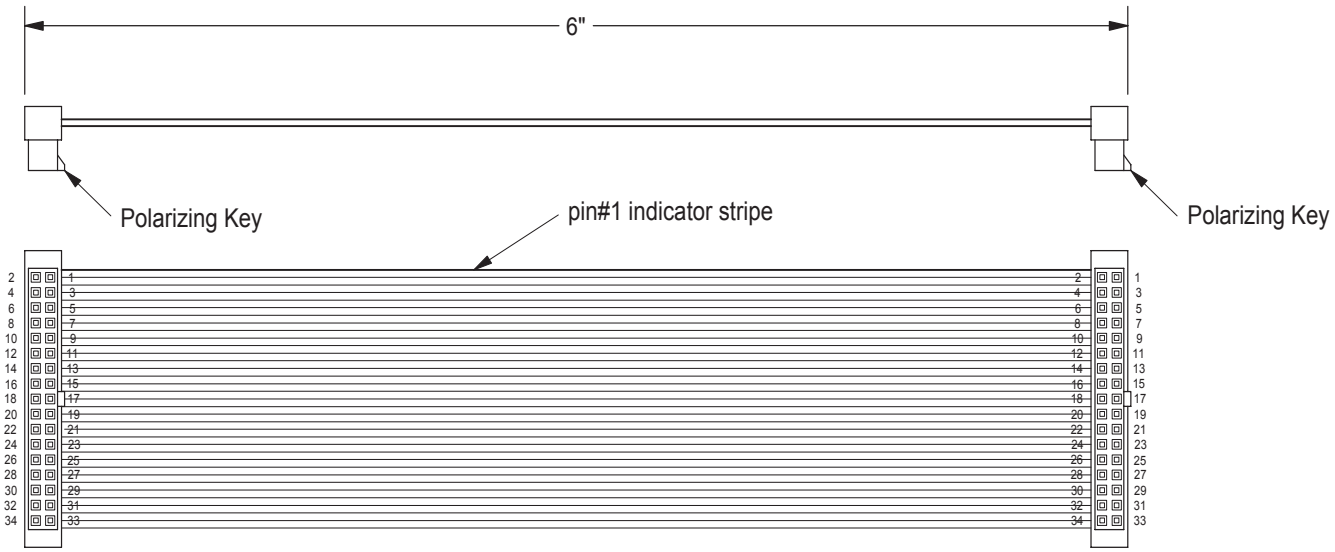

Notes:

1. Ribbon cable – 34-conductor, 1.0 mm centers round conductor flat cable, 28AWG (7x36) stranded copper conductors; gray PVC with pin #1 edge marked.
2. 2 mm ribbon, female polarized connectors – IDC connection to ribbon, contacts are beryllium copper plated with 30 micro inches gold plating over 50 micro inches nickel, connectors mate to 0.5 mm square posts on 2 mm centers.

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Figure 6: **Ribbon Cable Diagrams**

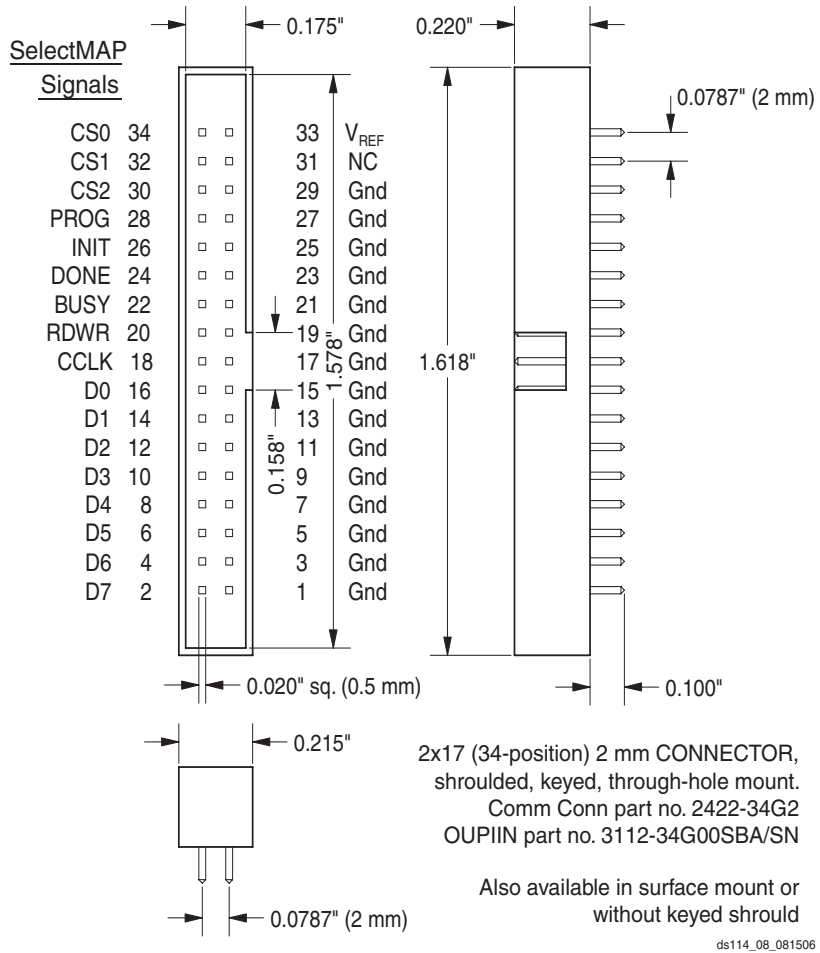

Figure 7: **Target Interface 34-Pin Connector Signal Assignments**

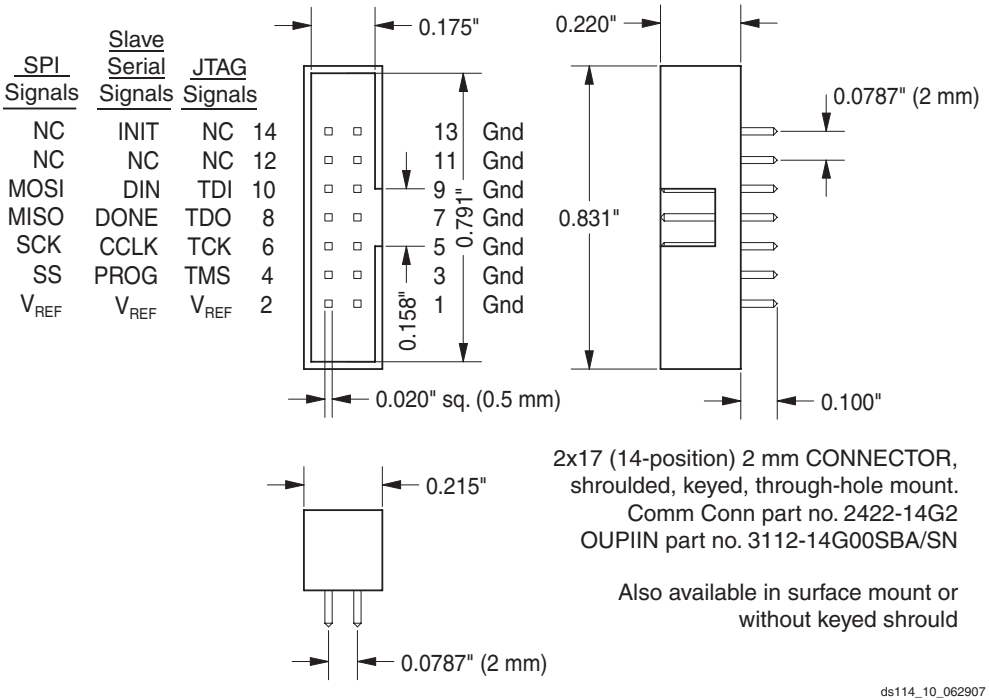

Figure 8: **Target Interface 14-Pin Connector Signal Assignments**

Table 3 lists some third-party sources for mating connectors for 2 mm pitch, 14-conductor ribbon cable.

Table 3: **Mating Connectors for 2 mm pitch, 14 Conductor Ribbon Cable**

Manufacturer	Part Number
Comm Con	2422-14G2
OUPIIN	3112-14G00SBA/SN

Notes:

1. Also available in surface mount or without keyed shroud.
2. Some manufacturer's pin assignments do not conform to Xilinx pin assignments. Please refer to the manufacturer's data sheet for more information.
3. Additional 14-pin ribbon cables can be purchased separately from the Xilinx Online Store.

Table 4 lists third-party sources for mating connectors for 2 mm pitch, 34-conductor ribbon cable.

Table 4: **Mating Connectors for 2 mm pitch, 34 Conductor Ribbon Cable**

Manufacturer	Part Number
Comm Con	2422-34G2
OUPIIN	3112-34G00SBA/SN

Notes: Also available in surface mount or without keyed shroud.

Interface Pin Descriptions

The interface pins for the Serial/JTAG/SPI, SelectMAP, and adapter ports are described in Table 5, Table 6, and Table 7, respectively.

Table 5: **SS/JTAG/SPI Port: 14-Pin Ribbon Cable Connector**

Ribbon Cable Number	Slave-Serial Configuration Mode	JTAG Configuration Mode	SPI(2) Programming Mode	Type	Description
2	V_{REF}	V_{REF}	V_{REF}	In	**Target Reference Voltage.**(3) This pin should be connected to a voltage bus on the target system that serves the JTAG, slave-serial interface. or SPI. For example, when programming a Coolrunner-II device using the JTAG port, V_{REF} should be connected to the target V_{AUX} bus.
4	PROG	–	–	Out	**Configuration Reset.** This pin is used to force a reconfiguration of the target FPGA(s). It should be connected to the PROG_B pin of the target FPGA for a single-device system, or to the PROG_B pin of all FPGAs in parallel in a daisy-chain configuration.
6	CCLK	–	–	Out	**Configuration Clock.** FPGAs load one configuration bit per CCLK cycle in slave-serial mode. CCLK should be connected to the CCLK pin on the target FPGA for a single-device configuration, or to the CCLK pin of all FPGAs in parallel in a daisy-chain configuration.
8	DONE	–	–	In	**Configuration Done.** This pin indicates to MultiPRO tool that target FPGAs have received the entire configuration bitstream. It should be connected to the Done pin on all FPGAs in parallel for daisy-chained configurations. Additional CCLK cycles are issued following the positive transition of Done to insure that the configuration process is complete.
10	DIN	–	–	Out	**Configuration Data Input.** This is the serial input data stream for target FPGAs. It should be connected to the DIN pin of the target FPGA in a single-device system, or to the DIN pin of the first FPGA in a daisy-chain configuration.
12	N/C	N/C	N/C	Out	**Test Driver.** This pin is reserved for Xilinx diagnostics and should not be connected to any target circuitry.
14	INIT	N/C	N/C	BIDIR	**Configuration Initialize.** This pin indicates that configuration memory is being cleared. It should be connected to the INIT_B pin of the target FPGA for a single-device system, or to the INIT_B pin on all FPGAs in parallel in a daisy-chain configuration.

Table 5: **SS/JTAG/SPI Port: 14-Pin Ribbon Cable Connector *(Cont'd)***

Ribbon Cable Number	Slave-Serial Configuration Mode	JTAG Configuration Mode	SPI(2) Programming Mode	Type	Description
4	–	TMS	–	Out	**Test Mode Select.** This is the JTAG mode signal that establishes appropriate TAP state transitions for target ISP devices. It should be connected to the TMS pin on all target ISP devices that share the same data stream.
6	–	TCK	–	Out	**Test Clock**. This is the clock signal for JTAG operations, and should be connected to the TCK pin on all target ISP devices that share the same data stream.
8	–	TDO	–	In	**Test Data Out**. This is the serial data stream received from the TDO pin on the last device in a JTAG chain.
10	–	TDI	–	Out	**Test Data In**. This is the serial data stream transmitted to the TDI pin on the first device in a JTAG chain.
4	–	–	SS	Out	**SPI Select.** This pin is the active-Low SPI chip select signal. This should be connected to the S(2) pin on the SPI flash PROM.
6	–	–	SCK	Out	**SPI Clock.** This pin is the clock signal for SPI operations and should be connected to the C(2) pin on the SPI flash PROM.
8	–	–	MISO	In	**SPI Master-Input, Slave-Output.** This pin is the target serial output data stream for SPI operations and should be connected to the Q(2) pin on the SPI flash PROM.
10	–	–	MOSI	Out	**SPI Master-Output Slave-Input.** This pin is the target serial input data stream for SPI operations and should be connected to the D(2) pin on the SPI flash PROM.
1, 3, 5, 7, 9, 11, 13	–	–	–	–	**Digital Ground**.(1)

Notes:

1. All odd pins (1, 3, 5, 7, 9, 11, and 13) should be connected to digital ground on the target end of the ribbon cable. Minimum crosstalk is achieved when using all grounds.
2. The listed SPI pin names match those of SPI flash memories from STMicroelectronics. Pin names of compatible SPI devices from other vendors can be different. Consult the vendor's SPI device data sheet for corresponding pin names.
   Caution! The PROG_B pin of the FPGA, which is connected to a target SPI device, must be asserted Low during SPI programming to ensure the FPGA does not contend with the SPI programming operation.
3. The target reference voltage must be regulated and must not have a current-limiting resistor in series with the V_{REF} pin.

Table 6: **SelectMAP Port: 34-Pin Ribbon Cable Connector Interface Pin Descriptions**

Ribbon Cable Pin Number	SelectMAP Configuration Mode	Type	Description
16	D0	BIDIR	Byte-Wide Data Bus, Bit 0
14	D1	BIDIR	Byte-Wide Data Bus, Bit 1
12	D2	BIDIR	Byte-Wide Data Bus, Bit 2
10	D3	BIDIR	Byte-Wide Data Bus, Bit 3
8	D4	BIDIR	Byte-Wide Data Bus, Bit 4
6	D5	BIDIR	Byte-Wide Data Bus, Bit 5
4	D6	BIDIR	Byte-Wide Data Bus, Bit 6
2	D7	BIDIR	Byte-Wide Data Bus, Bit 7
18	CCLK	OUT	Configuration Clock
20	RDWR	OUT	Configuration Read / Write Control
22	BUSY	IN	Configuration Flow Control
24	DONE	IN	Configuration Done
26	INIT	BIDIR	Configuration Initialize

Table 6: **SelectMAP Port: 34-Pin Ribbon Cable Connector Interface Pin Descriptions *(Cont'd)***

Ribbon Cable Pin Number	SelectMAP Configuration Mode	Type	Description
28	PROG	OUT	Configuration Reset
30	CS2	OUT	Chip Select 2
32	CS1	OUT	Chip Select 1
34	CS0	OUT	Chip Select 0
33	V_{REF}	IN	Target reference voltage
31	NC	–	No Connection
1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29	Gnd	–	Digital Ground

Table 7: **Adapter Port: 20-Pin DIN Connector Interface Pin Descriptions**

DIN Pin Number	JTAG Configuration Mode	Type	Description
A8	TCK	OUT	**Test Clock.** This is the clock signal for JTAG operations. It is connected to the 'TCK' pin on the adapter socket.
A2	TMS	OUT	**Test Mode Select.** This is the JTAG mode signal that establishes appropriate TAP state transitions for the target device. It is connected to the 'TMS' pin on the adapter socket.
A4	TDI	OUT	**Test Data In.** This is the serial input data stream for JTAG operations and is connected to the 'TDI' pin on the adapter socket.
A6	TDO	IN	**Test Data Out.** This is the serial output data stream for JTAG operations and is connected to the 'TDO' pin on the adapter socket.
A1	PEN	OUT	**Port Enable.** Reserved for future applications.
B4	ID1	IN	**Adapter ID1.** This is the high order bit for the automatic adapter identification circuit.
A3	ID0	IN	**Adapter ID0.** This is the low order bit for the automatic adapter identification circuit.
B1	V_{REF}	IN	**Adapter Reference Voltage.** This voltage is established by a local linear regulator on each device adapter according to the specifications of the device family.
B7, B8, B9, A10, B10	+5V DC	OUT	**Switched Supply Voltage.**
A9	EGND	–	**Safety Ground.**
A5, B5, B6, A7	GND	–	**Digital Ground.**

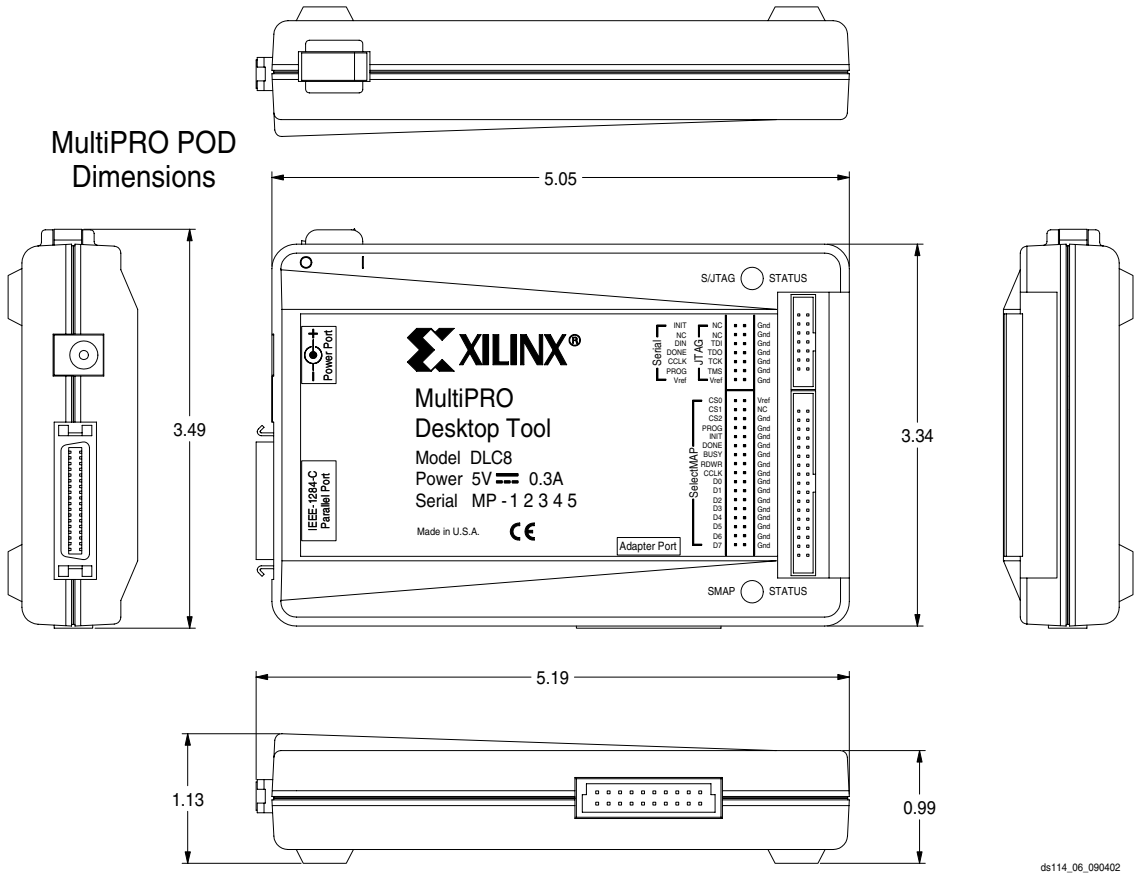

Figure 9: **MultiPRO Pod Dimensions (inches)**

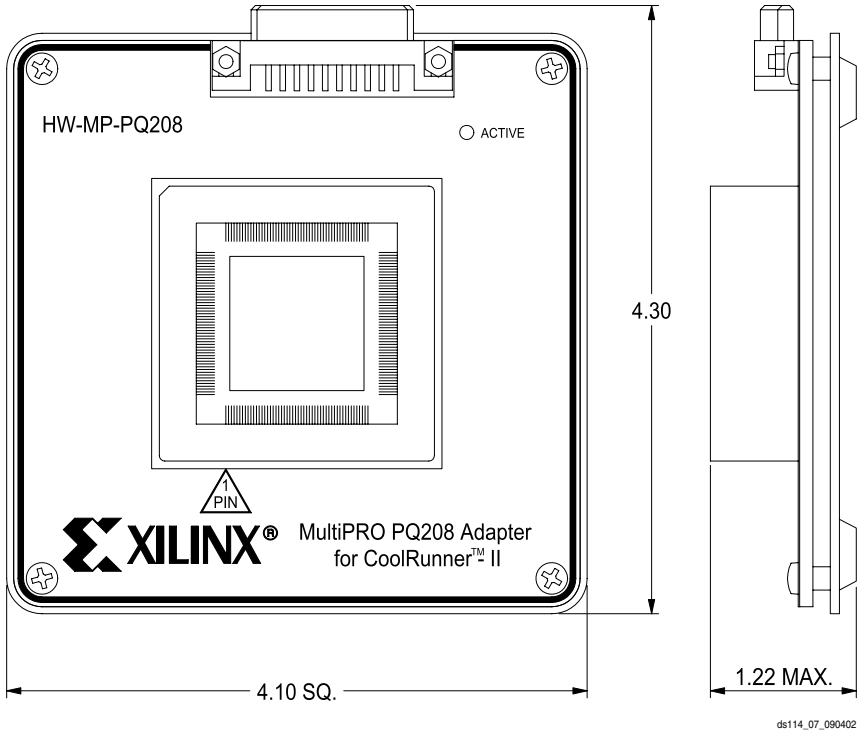

Figure 10: **Typical MultiPRO Adapter Dimensions (inches)**

Operating Characteristics

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	DC Supply Voltage	+6.0	V
T_A	Operating Temperature Range	0 to 70	°C
T_{STG}	Storage Temperature Range	–40 to +85	°C
P_D	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (Any Output)	±16	mA

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	DC Supply Voltage	External Power Supply	4.75	5.25	V
V_{REF}	Target Reference Voltage		1.5	5.5	V
I_{CC}	Operating Current		130	200	mA

Ordering Information

Part Number	Description
HW-MULTIPRO	MultiPRO Desktop Tool for US, Asia, Japan
HW-MULTIPRO-EC	MultiPRO Desktop Tool with European plug
HW-MULTIPRO-UK	MultiPRO Desktop Tool with UK plug
HW-MP-PC44-1	44-pin PLCC Adapter for XC18V00 PROMs
HW-MP-VQ44-1	44-pin VQFP Adapter for XC18V00 PROMs
HW-MP-VQ44-2	44-pin VQFP Adapter for CoolRunner-II CPLDs
HW-MP-CP56	56-ball Chip Scale Adapter for CoolRunner-II CPLDs
HW-MP-VQ100	100-pin VQFP Adapter for CoolRunner-II CPLDs
HW-MP-CP132	132-ball Chip Scale Adapter for CoolRunner-II CPLDs
HW-MP-SO20	20-pin SOIC Adapter for XC18V00 PROMs
HW-MP-PC20	20-pin PLCC Adapter for XC18V00 PROMs
HW-MP-PC44-2	44-pin PLCC Adapter for CoolRunner-II CPLDs
HW-MP-TQ144	144-pin TQFP Adapter for CoolRunner-II CPLDs
HW-MP-FT256	256-ball Fine Pitch Thin BGA Adapter for CoolRunner-II CPLDs
HW-MP-FG324	324-ball Fine Pitch BGA Adapter for CoolRunner-II CPLDs
HW-MP-PQ208	208-pin PQFP Adapter for CoolRunner-II CPLDs
HW-MP-V020	20-pin TSSOP Adapter for Platform Flash PROMs
HW-MP-FS48	48-ball Chip Scale BGA Adapter for Platform Flash PROMs
HW-MP-VO48	48-pin TSOP Adapter for Platform Flash PROMs
HW-MP-QF32	32-pin QFP Adapter for CoolRunner-II CPLDs
HW-MP-QF48	48-pin QFP Adapter for CoolRunner-II CPLDs

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/10/02	1.0	Initial Xilinx release.
12/24/02	1.1	Updated "Features", "Status Indicators", and "Adapter Port: 20-Pin DIN Connector Interface Pin Descriptions".
01/24/03	1.2	Updated "Features", "Device Adapters", Table 1, "Automatic Voltage Sensing", Table 7, and "Ordering Information".
04/10/03	1.3	Added list of supported Spartan-3 devices.
04/29/03	1.4	Added Platform Flash PROM family to "Desktop Device Programming", "MultiPRO Desktop Tool Description", and "Ordering Information". Added "XCF00S/P" to "Device Adapters".
09/29/04	1.5	• Added part numbers HW-MP-FS48 and HW-MP-VO48 to table in section "Ordering Information," page 11. • Section "External Power Supply," page 3: Changed specification of power supply.
01/04/06	1.6	• Updated supported list of Xilinx devices and added recommendation for product usage during development in section "In-System Programming/Configuration," page 1. • Added part numbers HW-MP-QF32 and HW-MP-QF48 to section "Ordering Information," page 11. • Updated OUPIIN part numbers in Figure 7, Figure 8, Table 3, and Table 4. • Promoted to Product Specification.
08/31/06	1.7	Updated the maximum download speed to 10 MHz and provided references to related firmware and software requirements.
08/09/07	1.8	Added support for SPI.
02/08/08	1.9	• Updated document template. • Added discontinuance notice to page 1.

Notice of Disclaimer

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