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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD

March 2016

FDMA410NZT

Ultra Thin N-Channel 1.5 V PowerTrench® MOSFET

20 V, 9.5 A, 23 mΩ

Features

- 0.55mm max package height MicroFET 2x2mm Package
- Max $r_{DS(on)}$ = 23 mΩ at V_{GS} = 4.5 V, I_D = 9.5 A
- Max $r_{DS(on)}$ = 29 mΩ at V_{GS} = 2.5 V, I_D = 8.0 A
- Max $r_{DS(on)}$ = 36 mΩ at V_{GS} = 1.8 V, I_D = 4.0 A
- Max $r_{DS(on)}$ = 60 mΩ at V_{GS} = 1.5 V, I_D = 2.0 A
- HBM ESD protection level > 1.5 kV (Note 3)
- RoHS Compliant

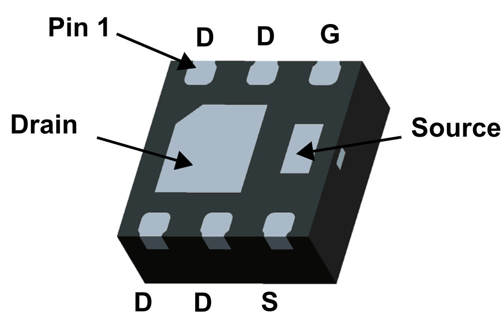
General Description

This Single N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced Power Trench process to optimize the $r_{DS(ON)}$ @ V_{GS} = 1.5 V on special MicroFET leadframe.

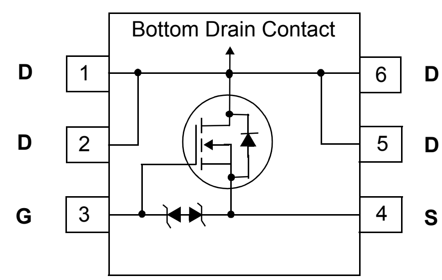
This design is similar to the FDMA410NZ, however it features our new advanced 0.55mm max 2x2 MLP package technology.

Applications

- Li-Ion Battery Pack
- Baseband Switch
- Load Switch
- DC-DC Conversion
- Mobile Device Switching



MicroFET 2X2 (Bottom View)



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	-Continuous T_A = 25 °C (Note 1a)	9.5	A
	-Pulsed (Note 4)	63	
P_D	Power Dissipation T_A = 25 °C (Note 1a)	2.4	W
	Power Dissipation T_A = 25 °C (Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

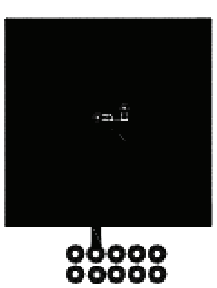
Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
410T	FDMA410NZT	MicroFET 2X2	7 ”	8 mm	3000 units

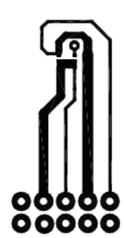
Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		15		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V			±10	μA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	0.4	0.8	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		–3		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 4.5 V, I_D = 9.5 A		14	23	mΩ
		V_{GS} = 2.5 V, I_D = 8.0 A		18	29	
		V_{GS} = 1.8 V, I_D = 4.0 A		25	36	
		V_{GS} = 1.5 V, I_D = 2.0 A		35	60	
		V_{GS} = 4.5 V, I_D = 9.5 A, T_J = 125 °C		21	32	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 9.5 A		36		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		935	1310	pF
C_{oss}	Output Capacitance			122	170	pF
C_{rss}	Reverse Transfer Capacitance			84	118	pF
R_g	Gate Resistance	f = 1 MHz	0.1	1.4	3.0	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 10 V, I_D = 9.5 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		8.5	17	ns
t_r	Rise Time			3.0	10	ns
$t_{d(off)}$	Turn-Off Delay Time			27	44	ns
t_f	Fall Time			3.3	10	ns
Q_g	Total Gate Charge	V_{GS} = 4.5 V , V_{DD} = 10 V, I_D = 9.5 A		10	14	nC
Q_{gs}	Gate to Source Charge			1.2		nC
Q_{gd}	Gate to Drain "Miller" Charge			2.0		nC
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.0	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.0 A (Note 2)		0.7	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 9.5 A, di/dt = 100 A/μs		16	30	ns
Q_{rr}	Reverse Recovery Charge			4.5	10	nC

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JA}$ is determined by the user's board design.



a. 52 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 145 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 ms, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
4. Pulsed Id please refer to Fig.11 SOA curve for more details.

Typical Characteristics T_J = 25 °C unless otherwise noted

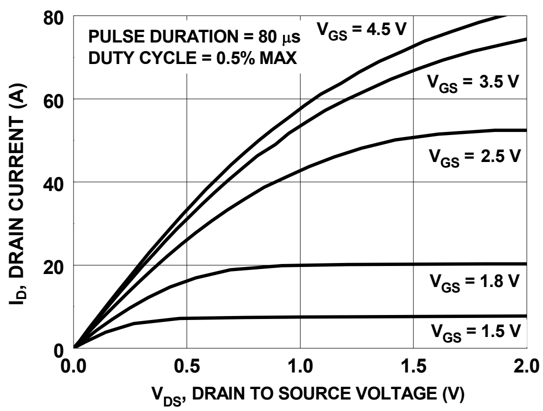


Figure 1. On Region Characteristics

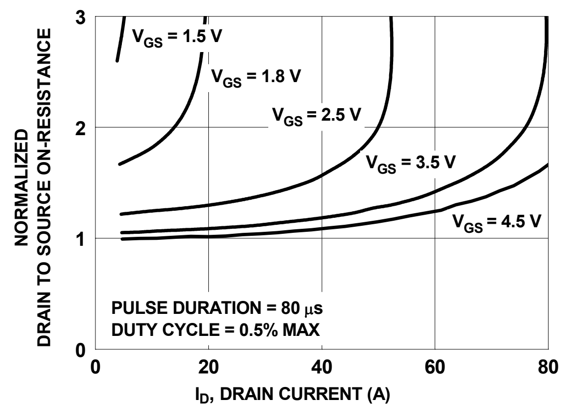


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

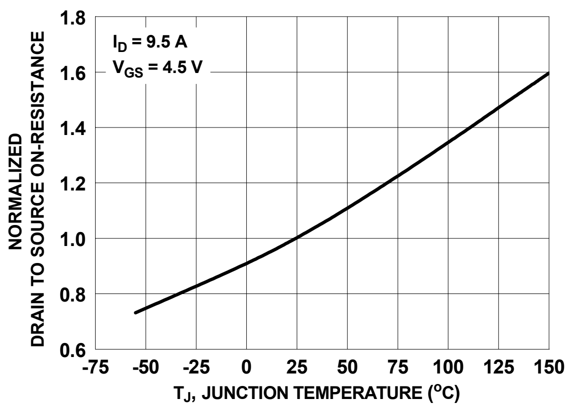


Figure 3. Normalized On Resistance vs Junction Temperature

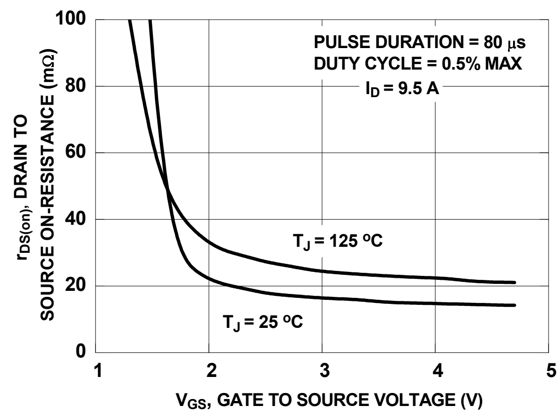


Figure 4. On-Resistance vs Gate to Source Voltage

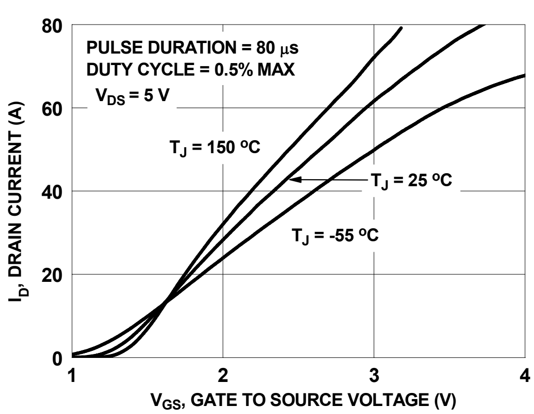


Figure 5. Transfer Characteristics

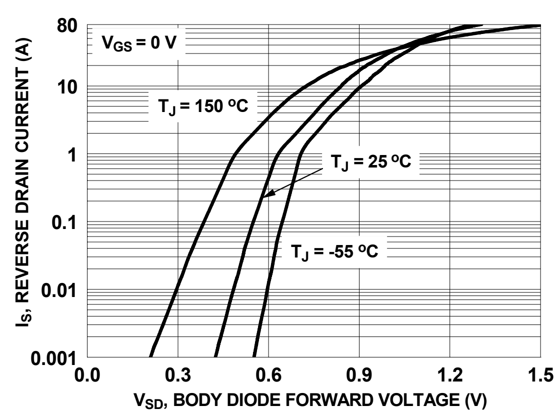


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

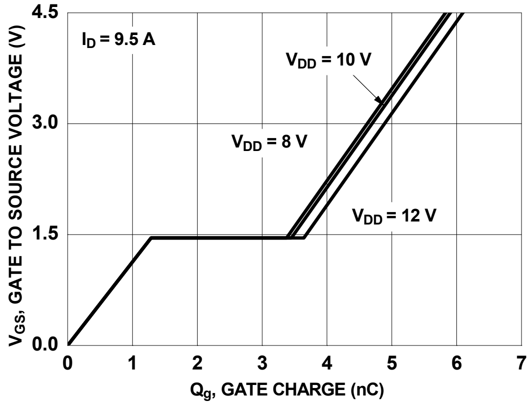


Figure 7. Gate Charge Characteristics

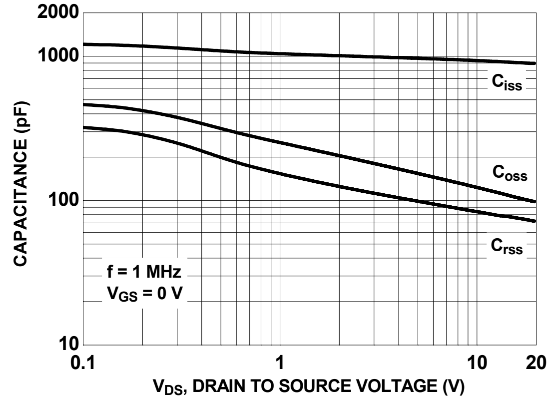


Figure 8. Capacitance vs Drain to Source Voltage

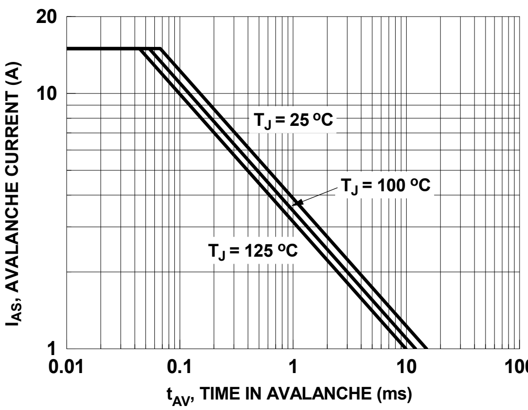


Figure 9. Unclamped Inductive Switching Capability

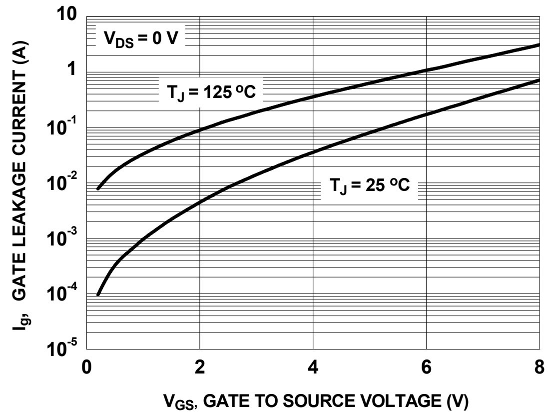


Figure 10. Gate Leakage Current vs Gate to Source Voltage

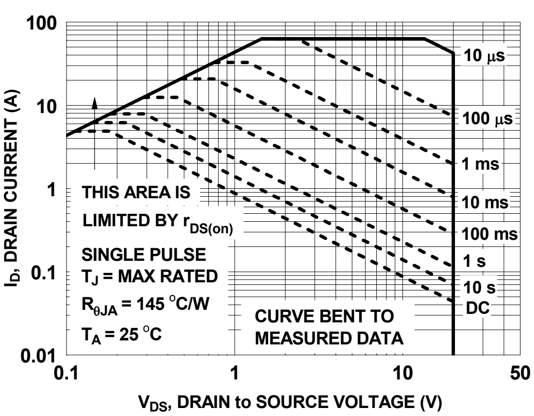


Figure 11. Forward Bias Safe Operating Area

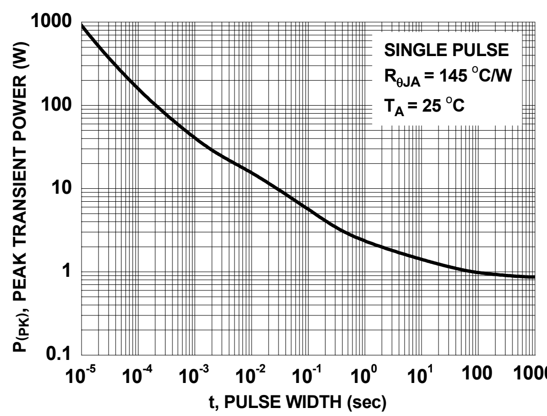


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

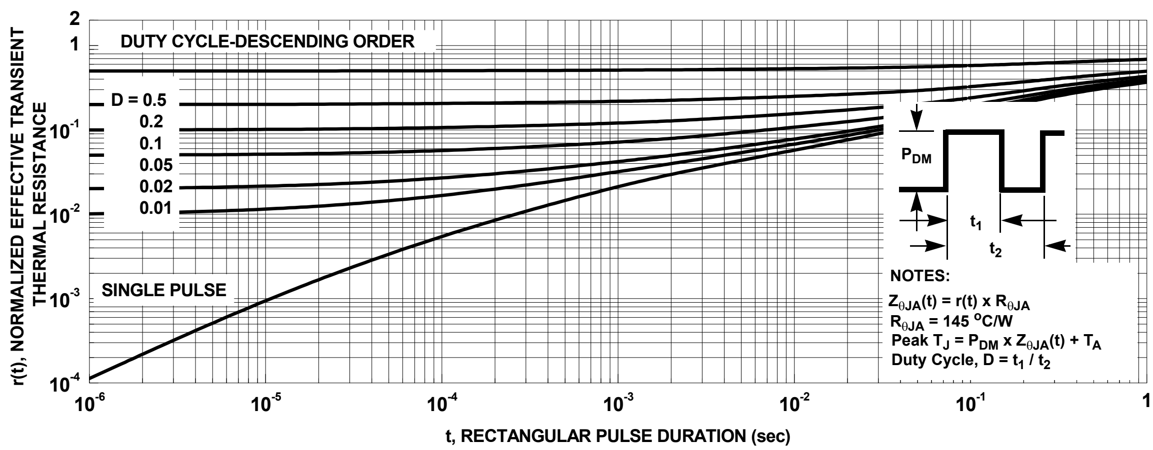
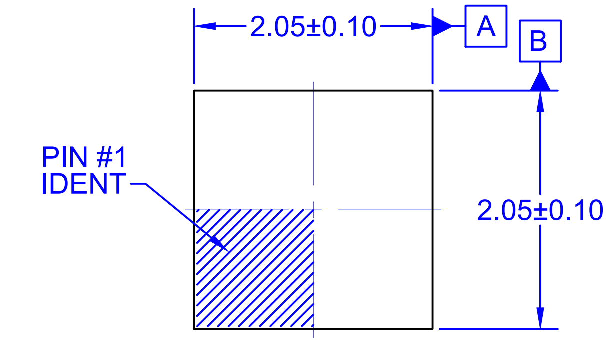
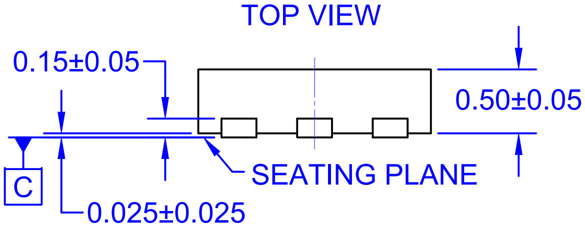


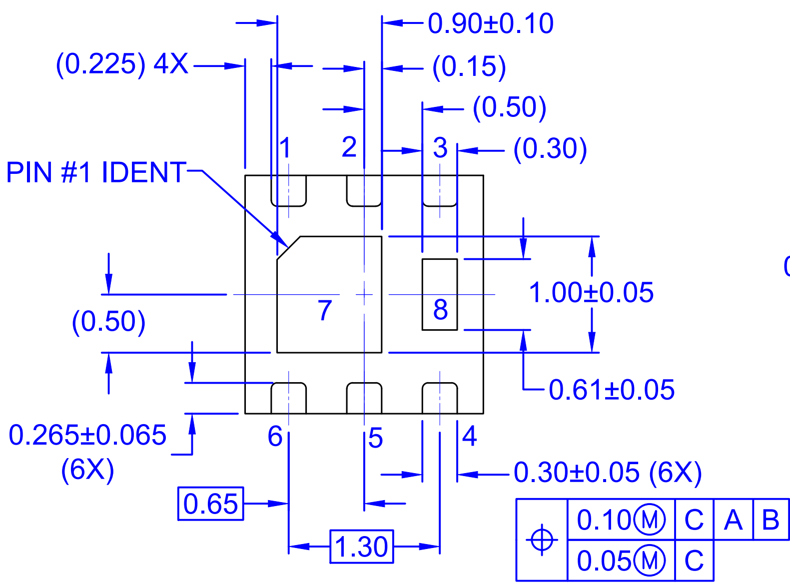
Figure 13. Junction-to-Case Transient Thermal Response Curve



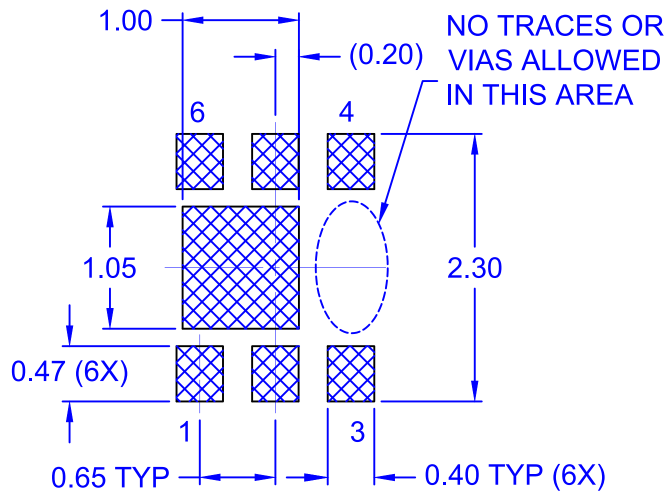
TOP VIEW



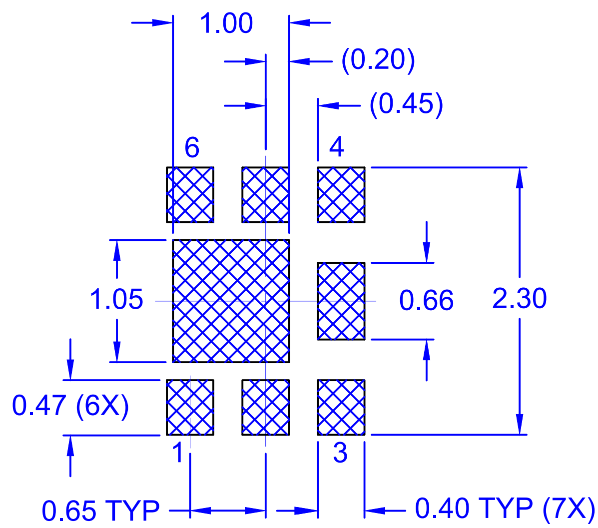
SIDE VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN OPT 1



RECOMMENDED LAND PATTERN OPT 2

NOTES:

A. PACKAGE DOES NOT CONFORM TO ANY JEDEC STANDARD.

B. DIMENSIONS ARE IN MILLIMETERS.

C. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

D. DRAWING FILENAME: MKT-FR015L3TrevB.

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